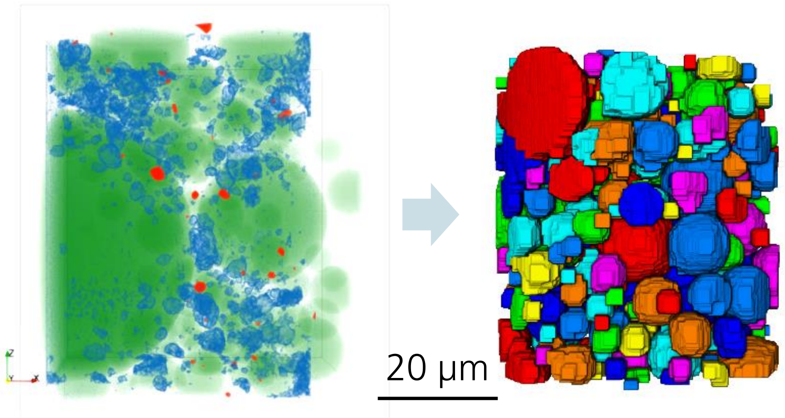
Fraunhofer Institute for Ceramic
Technologies and Systems IKTS

IRSP 2023, April 24-26, Bad Schandau, Germany

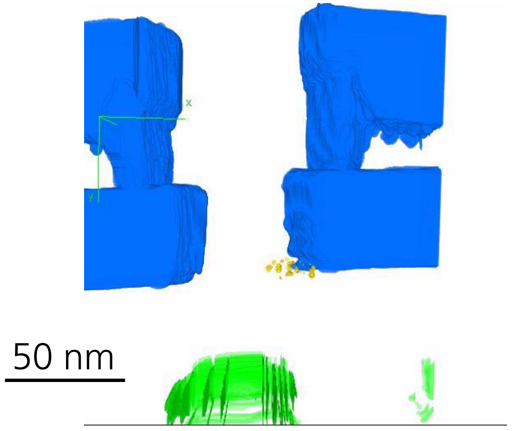
Piezoresistive Characteristics of MOSFET Channels Determined with Indentation Stress-induced Ring Oscillator Parameter Shifts

André Clausner, Simon Schlipf, Jens Paul, Simone Capecchi, Christoph Sander, and Ehrenfried Zschech

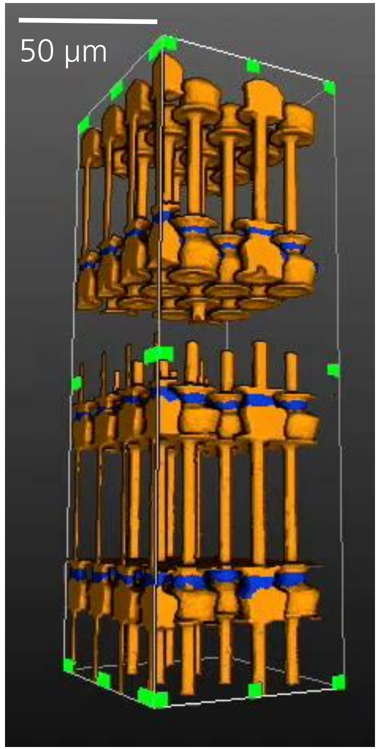
3D nanoanalytics @IKTS



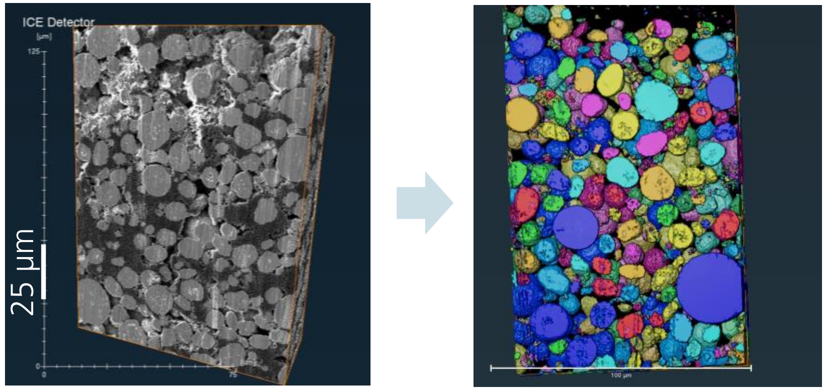
3D nXCT image of a microelectronics packaging material incl. 3D statistics



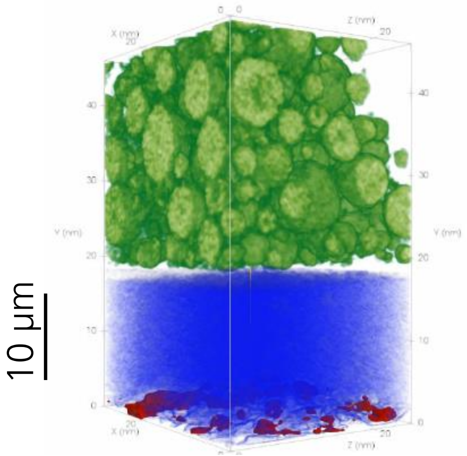
TEM tomography of a TDDB breakdown in a microelectonics MoL structure



3D nXCT stacked image of a TSV array for advanced 3D microcelectonics integration

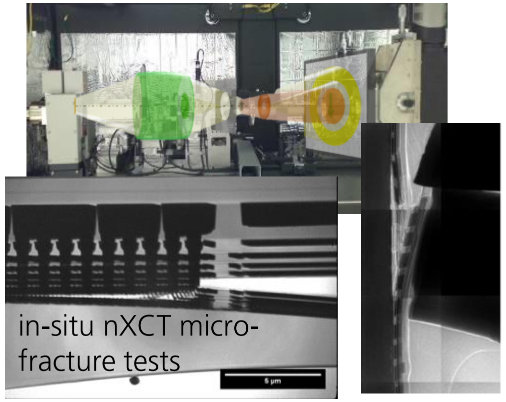


3D Plasma-FIB slice & view SEM image of a Li-Ion battery cathode material incl. 3D statistics



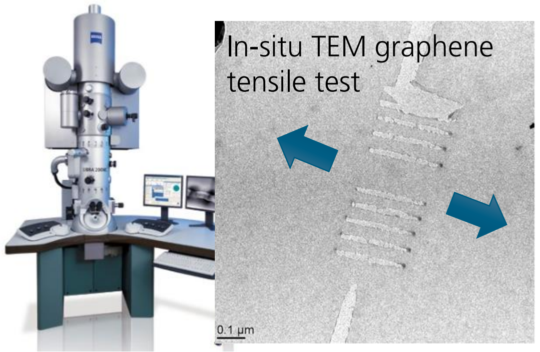
3D nXCT image of a battery cathode

Overview *in-situ* testing @ Fraunhofer IKTS



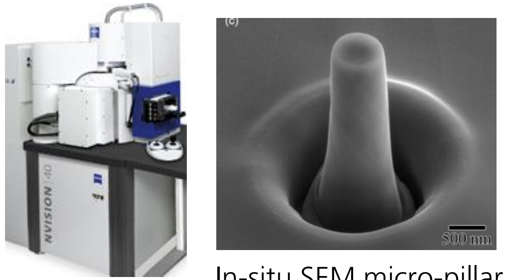
in-situ nXCT micro-fracture tests

In-Situ nXCT
nanomechanical testing



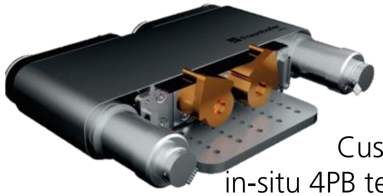
In-situ TEM graphene tensile test

In-Situ TEM
nanomechanical testing



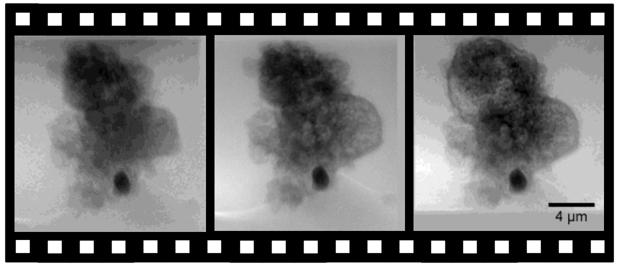
In-situ SEM micro-pillar compression

In-Situ SEM
nanomechanical testing



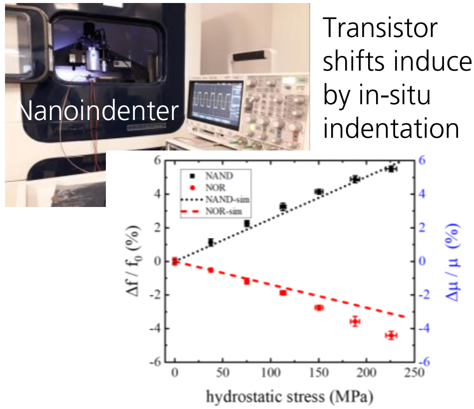
Custom
in-situ 4PB tester

Custom-build in-situ testing devices
for bending, tensile, compression, heating, cooling, etc.



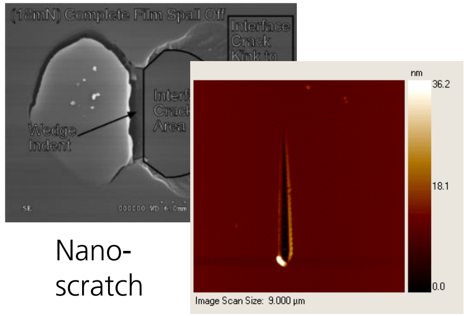
nano-XCT: in-situ Fe-Oxidation at 500°C

In-Situ nXCT
heating, battery cycling, chemical processes, …



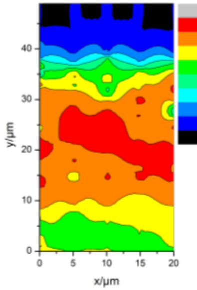
Transistor shifts induced by in-situ indentation

In-situ nanomechanical-electrical testing



Nano-scratch

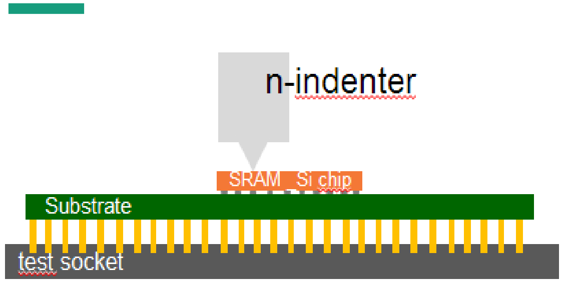
Micro-friction and **micro-fracture** characterization

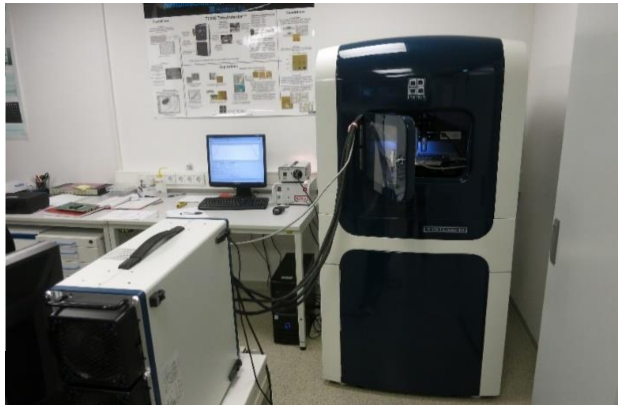


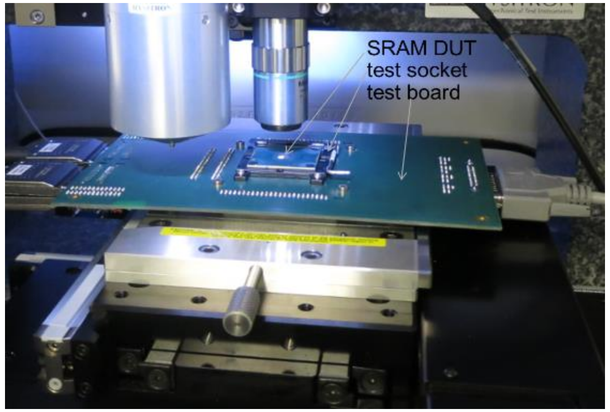
Young's modulus map

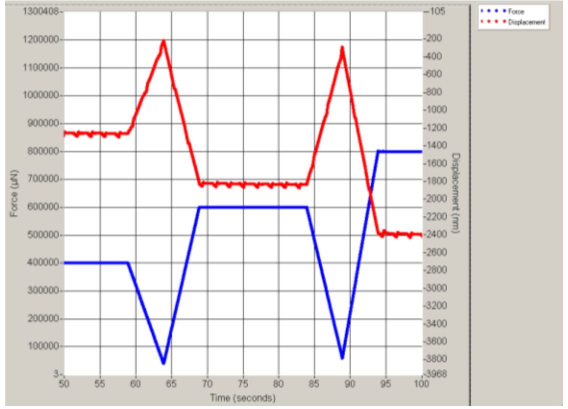
In-situ local property maps
Elasticity, Plasticity, strain-rate dependencies, …

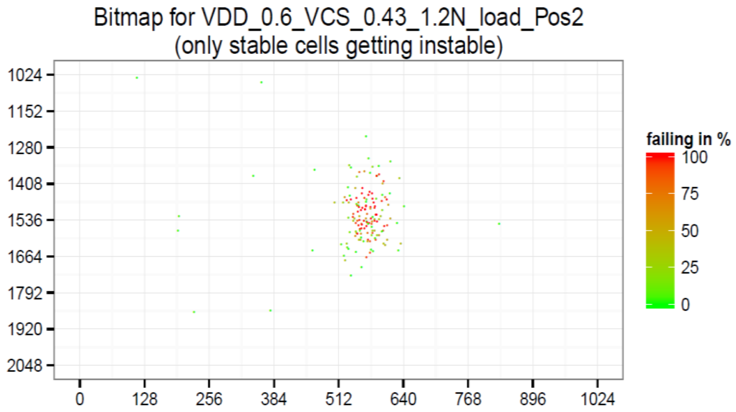
Mechanical testing at active SRAM cells

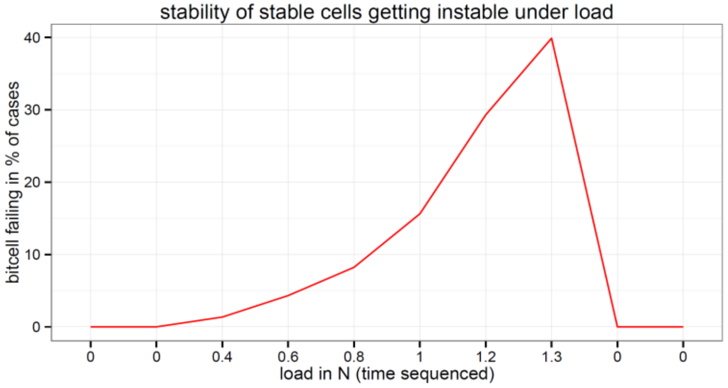


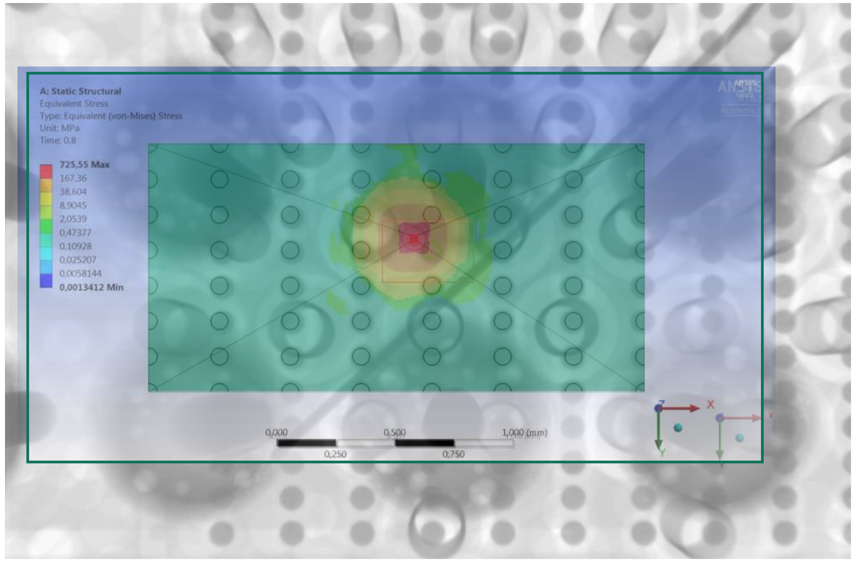






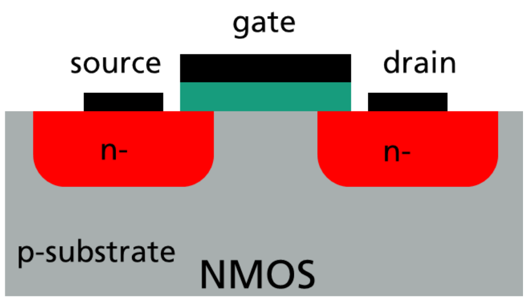


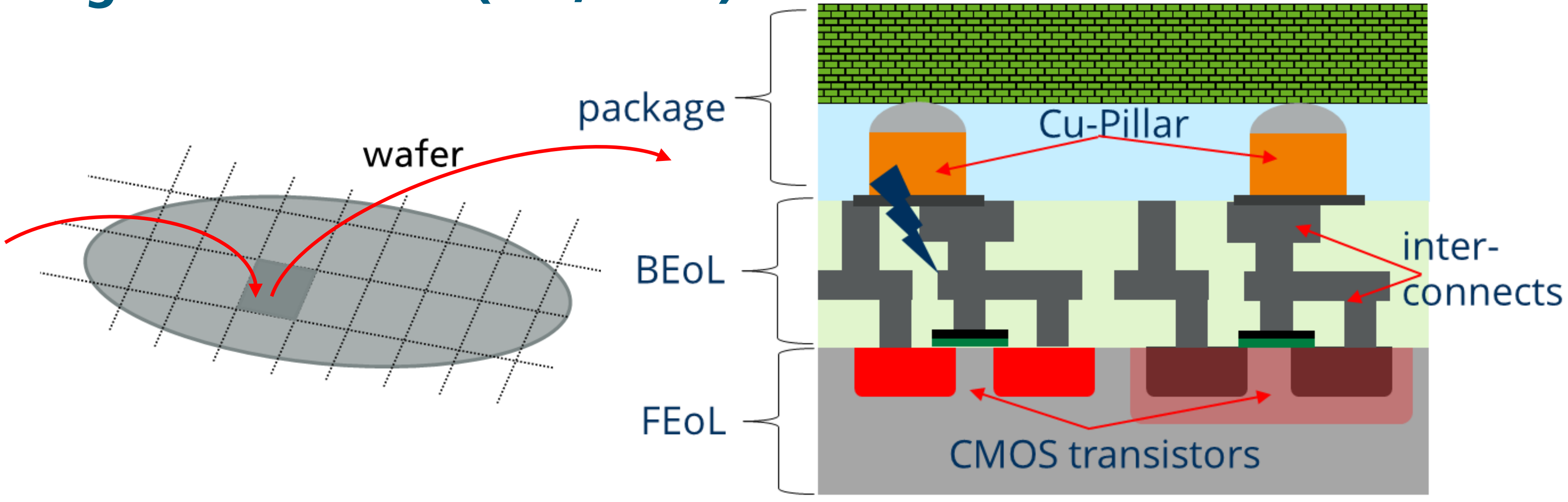




Clausner, Schlipf et al., Analysis of 28 nm SRAM Cell Stability Under Mechanical Load Applied by Nanoindentation, IRPS 2018

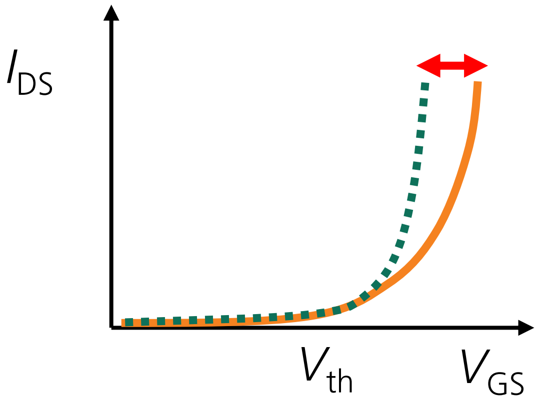
Motivation: Chip-package interaction (CPI, eCPI)





CMOS

N-type metal-oxide-semiconductor (NMOS)
P-type metal-oxide-semiconductor (PMOS)



Stress affects device characteristics

Chip-package interaction

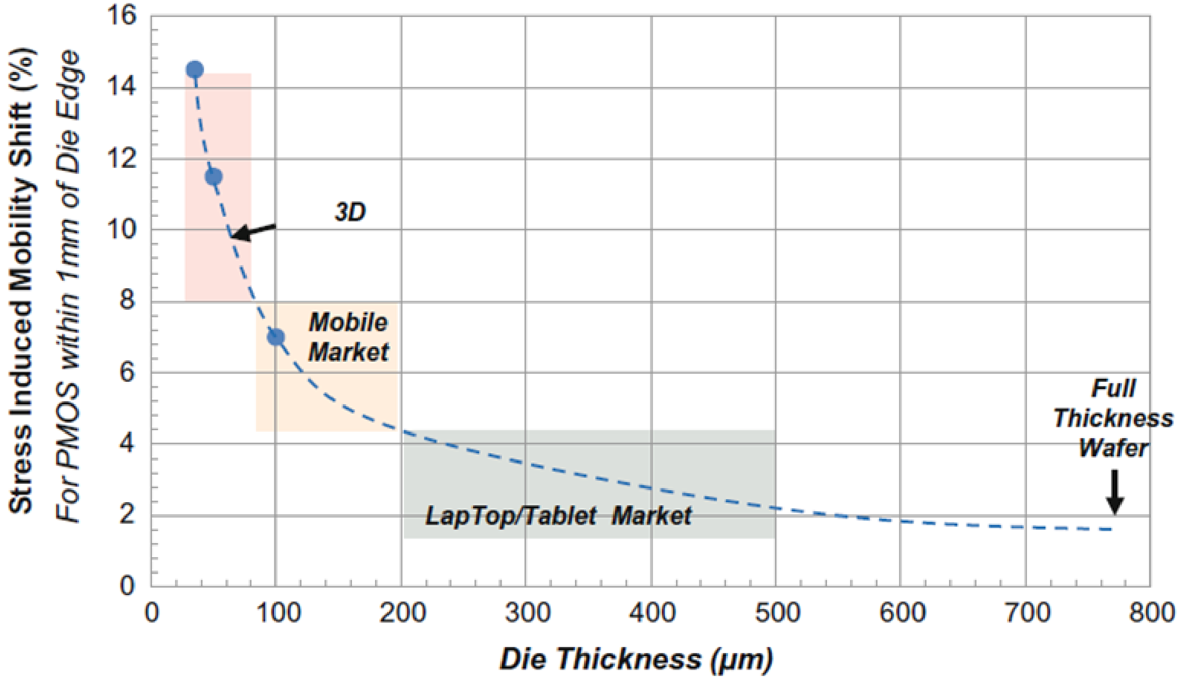
- Localized stress due to mismatch in the Coefficient of thermal expansion (CTE)
- Delamination in the BEoL
- **Shifts of the device performance → eCPI**

Motivation: Electrical Chip-package Interaction

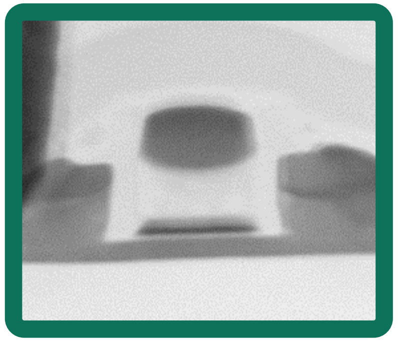
eCPI becomes more critical with 3D integration[1]

- Thinner chips
- More materials and interfaces
- Rigid interconnections (TSVs, Cu pillars …)

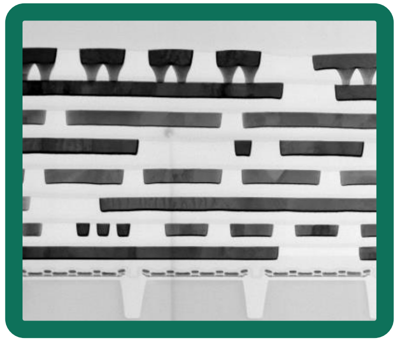
But: Electrical shifts difficult to detect



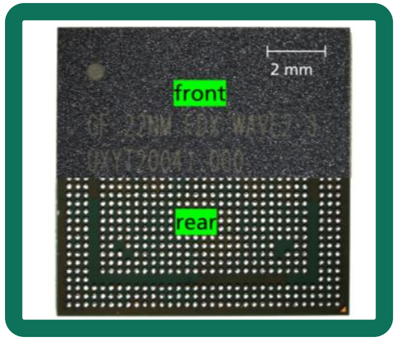
Stress induced mobility shifts[2]



transistor



BEoL



Flip - chip

nm *µm* *mm*

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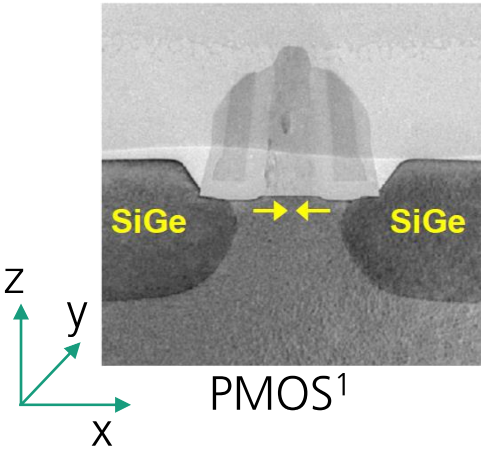
[1] Gonzalez, "Chip Package Interaction (CPI): Thermo Mechanical challenges in 3D Technologies"

[2] Radojcic, "More-than-Moore 2.5D and 3D SiP Integration"

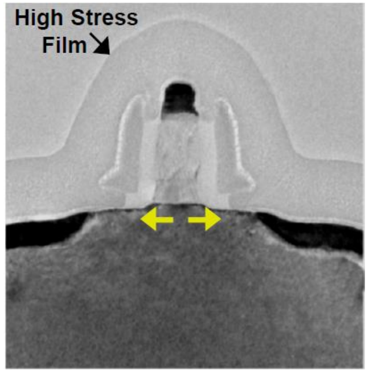
Motivation: Stress effects in silicon transistor channels

Stress effects on channel mobility[2]

- Stress direction (x, y, z), tensile or compressive
- Channel direction (x) and crystal orientation
- Devices (NMOS, PMOS)



PMOS[1]



NMOS[1]

Piezoresistive behavior[2]

(linearized mobility shift)

π-coefficients

$$\frac{\Delta\mu}{\mu_0} = \sigma_x \boldsymbol{\pi_x} + \sigma_y \boldsymbol{\pi_y} + \sigma_z \boldsymbol{\pi_z}$$

Effect of tensile stress (vice versa for compressive)[2]

Dir. of strain change	CMOS Performance	
	NMOS	PMOS
x	++	--
y	+	+
z	-	+

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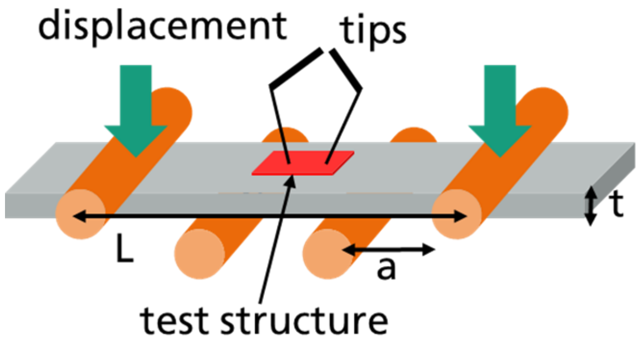
[1] Ghani et al. "A 90 nm High volume Manufacturing Logic Technology Featuring Novel 45nm Gate Length Strained Silicon CMOS Transistors"

[2] Thompson et al. "A 90-nm logic technology featuring strained-silicon"

Why indentation to study stress effects in microelectronic samples?

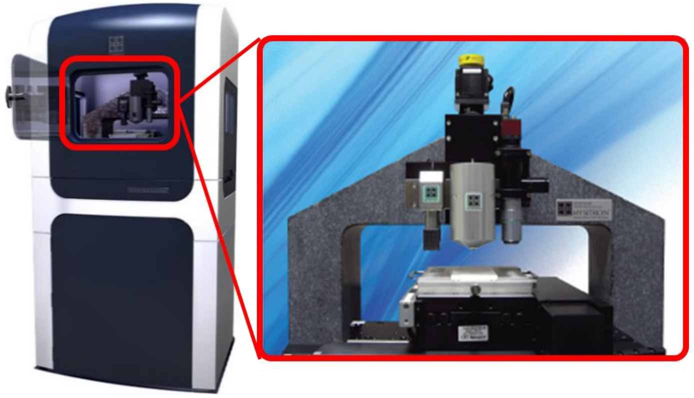


Four – point bending[1]

+ Uniaxial stress (σ_x or σ_y)

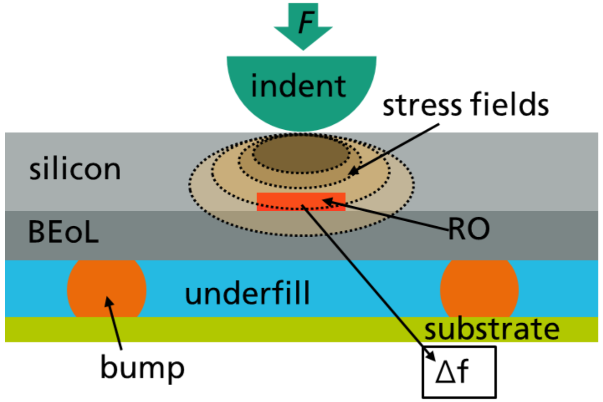
+ Piezoresistive coefficients

- Low stress (< 200 MPa)



Indentation[2,3]

- Precise transducers and stages
- Non-destructive loading
- Induce local stress



Indentation on flip chip packages

+ Localized stress effects (final chip)

+ Wide range of stress (MPa – GPa)

+ Control stress with varying the tip geometry (unconstrained contact)

+- 3D stress ($\sigma_x, \sigma_y, \sigma_z$)

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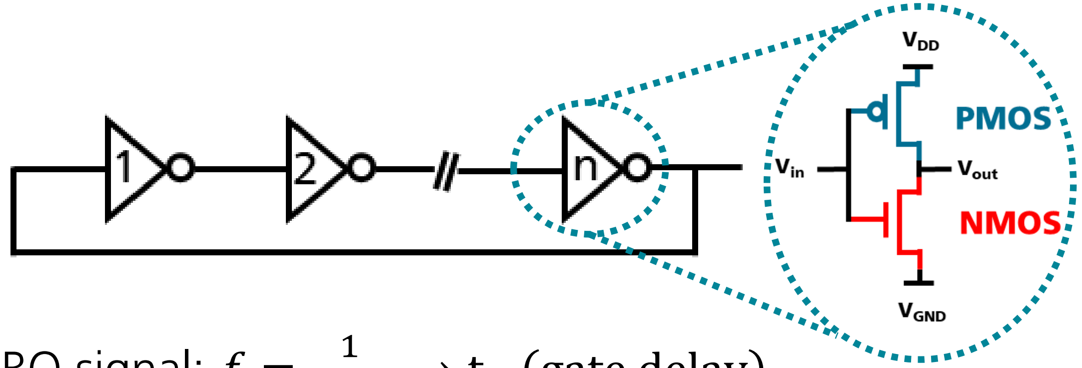
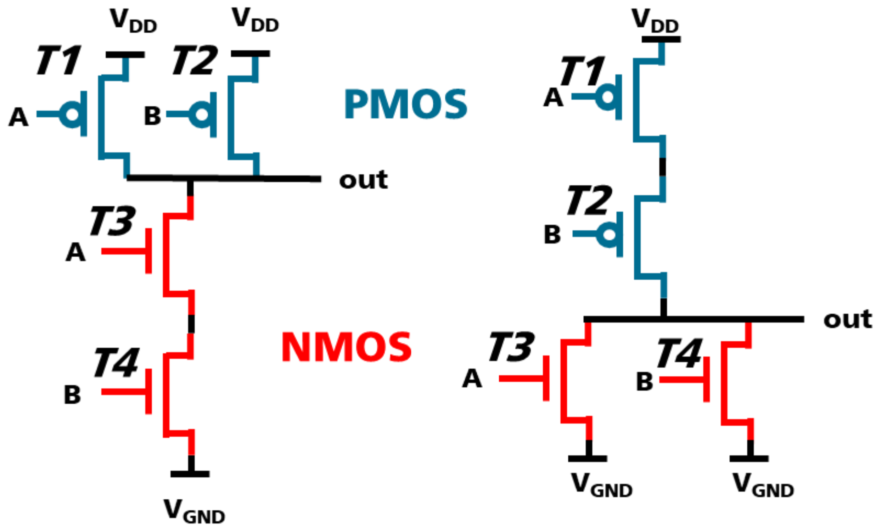
[1] Bradley et al. “ Piezoresistive Characteristics of Short-Channel MOSFETs on (100) Silicon”
[2] Liu et al., “In-situ Investigation of the Impact of Externally Applied Vertical Stress on III-V Bipolar Transistor”
[3] Clausner et al., “Analysis of 28 nm SRAM cell stability under mechanical load applied by nanoindentation”

Test structures: NAND – NOR ring oscillator (RO) sensor



RO signal: $f = \frac{1}{2nt_d} \rightarrow t_\mathrm{d}$ (gate delay)

Delay[1]: $t_d = \frac{C_L V_{DD}}{\mu C_{ox}\left(\frac{W}{L}\right)_n (V_{DD}-V_{th})^2}$



a) NAND gate **b) NOR gate**

RO – circuits (22 nm node)

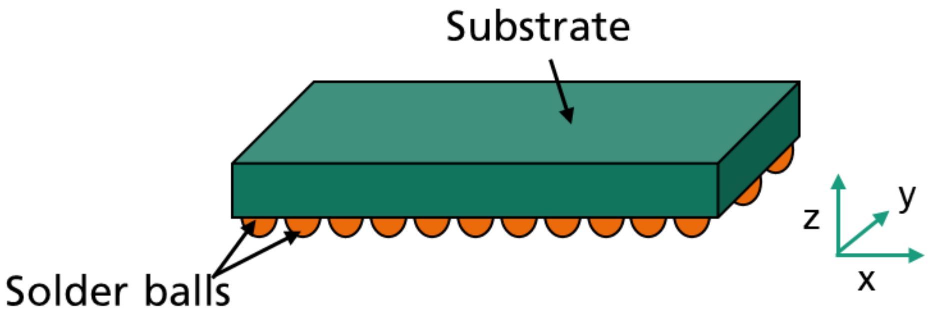
- Two independent RO (NAND & NOR)
- Both inputs connected and switched
- High statistics and sensitive (101 gates)
- Checkerboard configuration (10 x 10 μm²)

For RO operation:

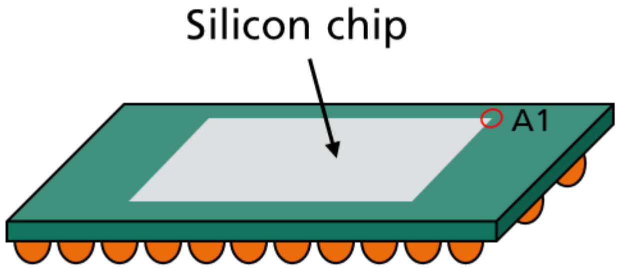
- NMOS : PMOS = 2 : 1 → **NAND**
- NMOS : PMOS = 1 : 2 → **NOR**

[1] N. H. E. Weste et al., *"CMOS VLSI design: A circuits and systems perspective"*

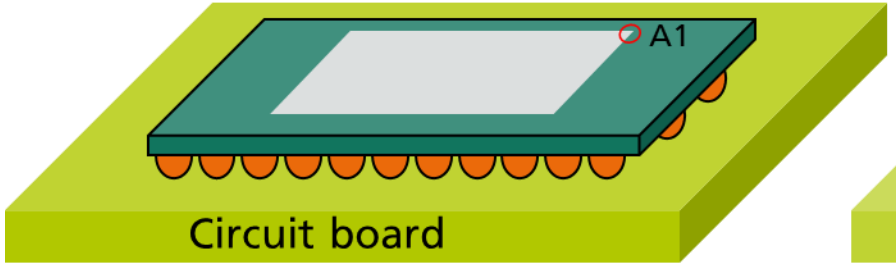
Sample preparation



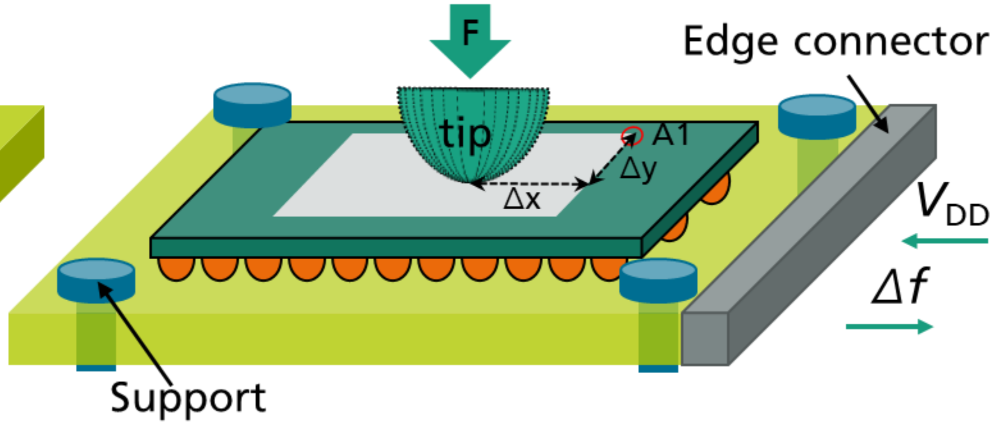
a) Flip chip sample



b) Reducing the thickness

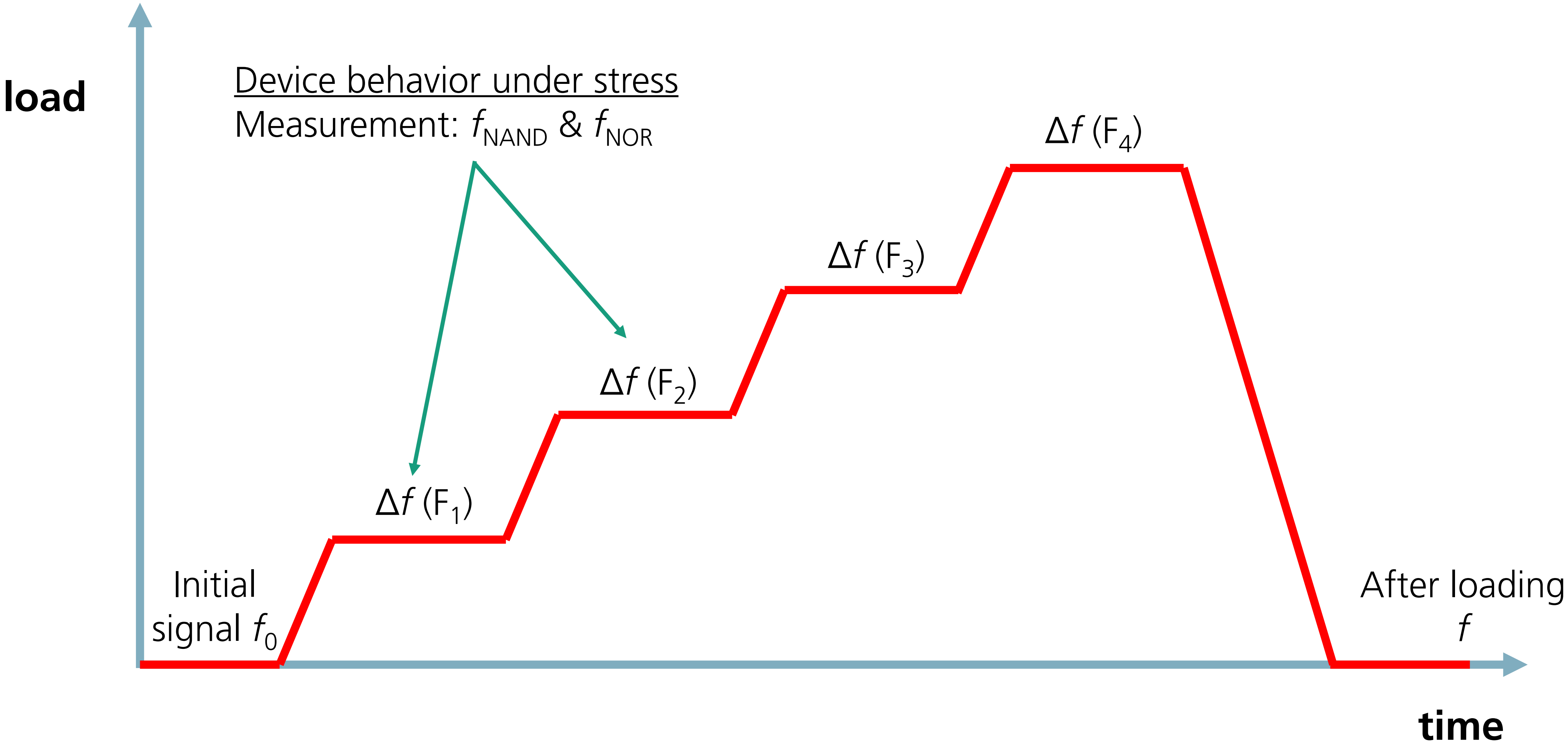


c) Electrical setup

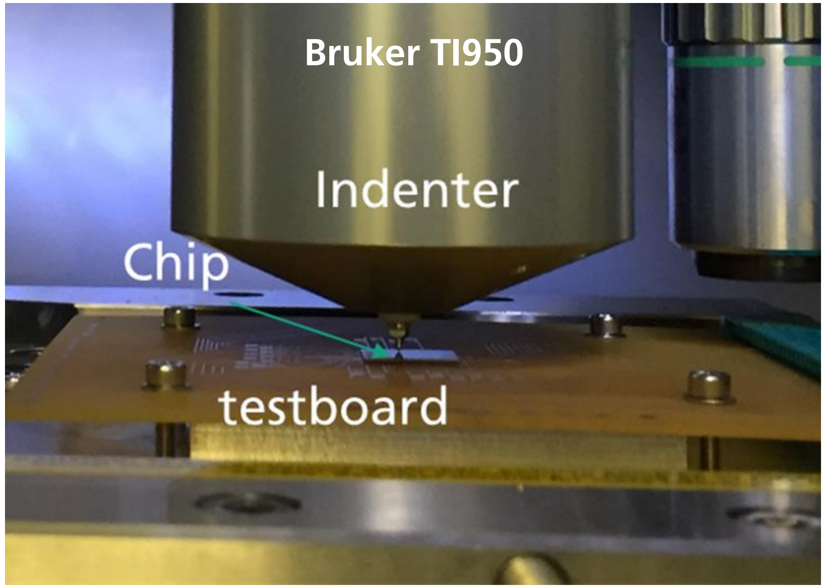


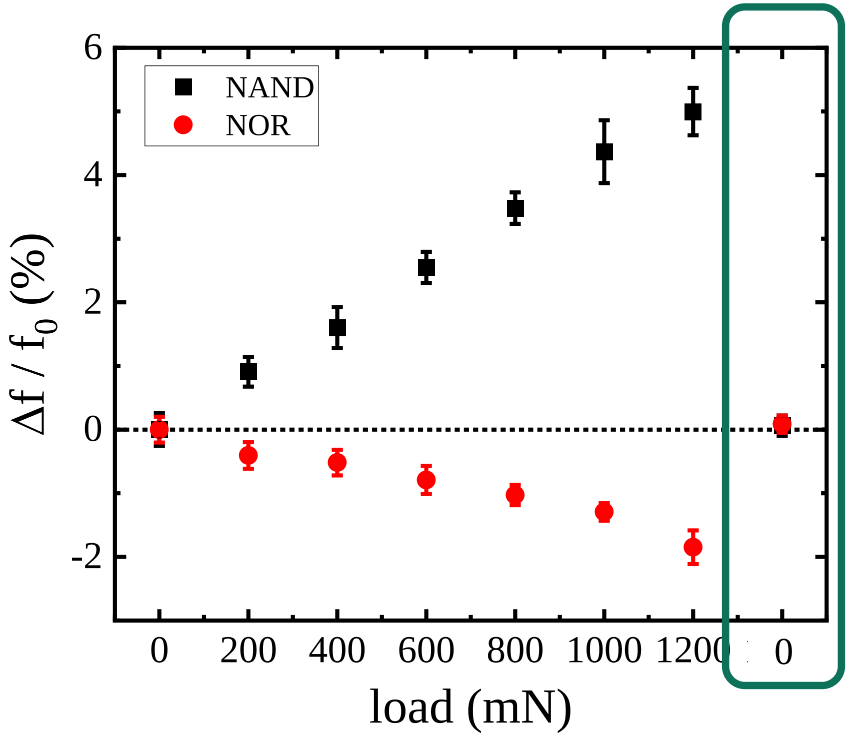
d) Mechanical – electrical testing

Mechanical – electrical testing routine



Experimental approach





Indentation experiments

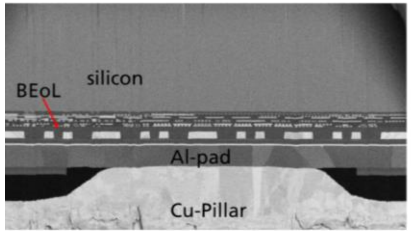
- Spherical tip (50 µm radius)
- Low contact stress
- Non-destructive material deformation

- NAND / NOR frequency shifts
- Approach consistent and reproducible

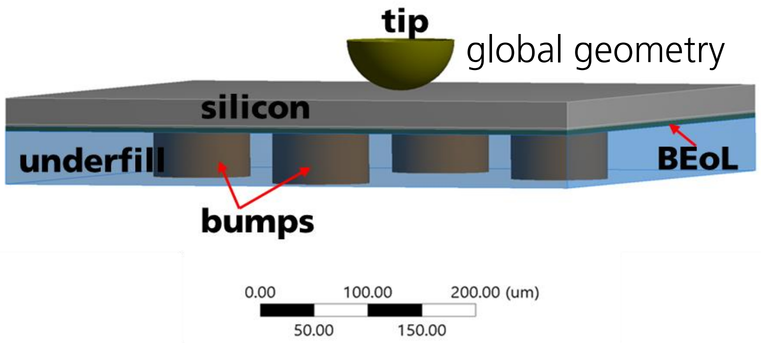
→ Stress required (direction and magnitude)

S. Schlipf et al., “Impact of Mechanical Strain on 22 nm FDSOI Device Performance using Nanoindentation,” *in 2019 IEEE IIRW*

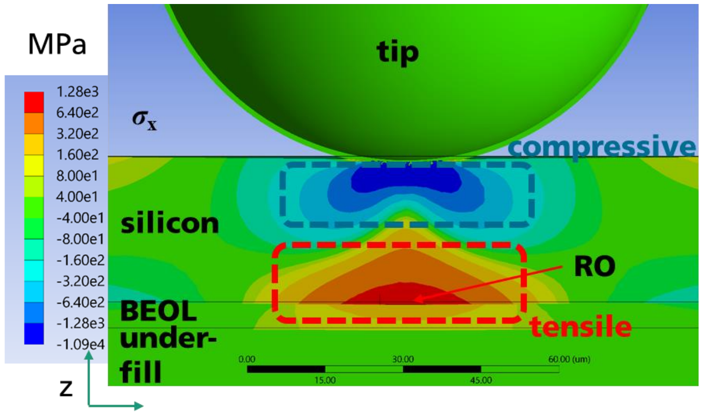
Finite element simulation: stress fields in the ROI

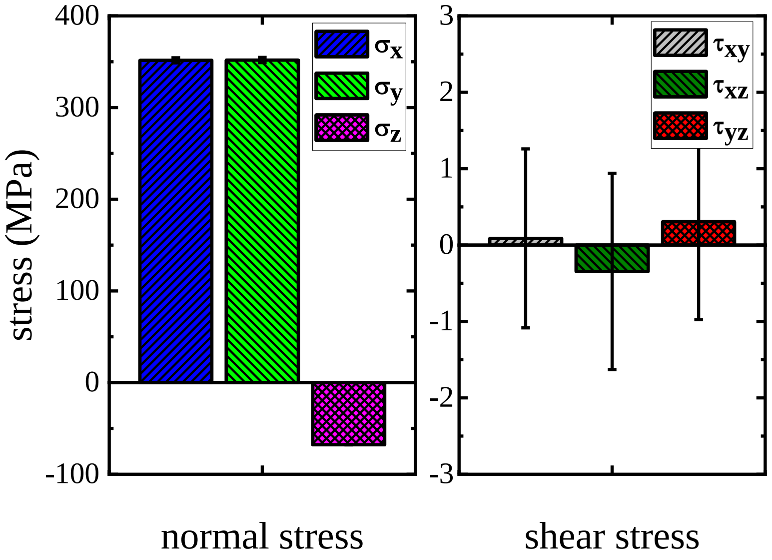


local geometry



global geometry





FE -analysis

- Submodel for every chip
- Geometry, chip layout, tip characteristics…
- Elastic material properties

Spherical tips

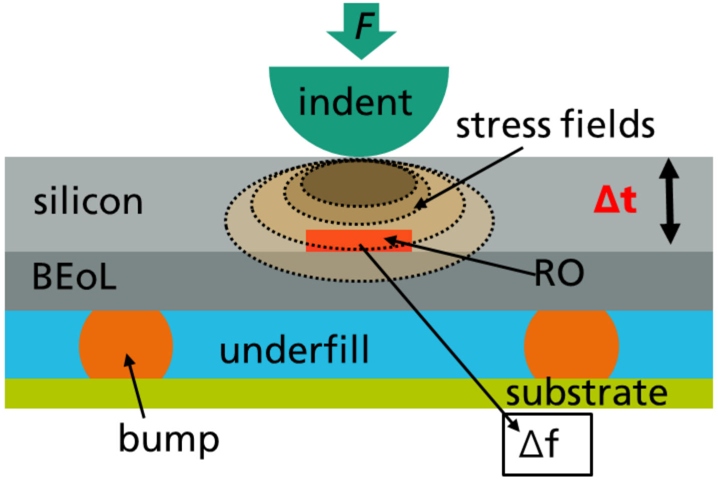
- Tensile stress in the ROI (x,y)
- Explained with stiff and compliant materials

Stress tensor

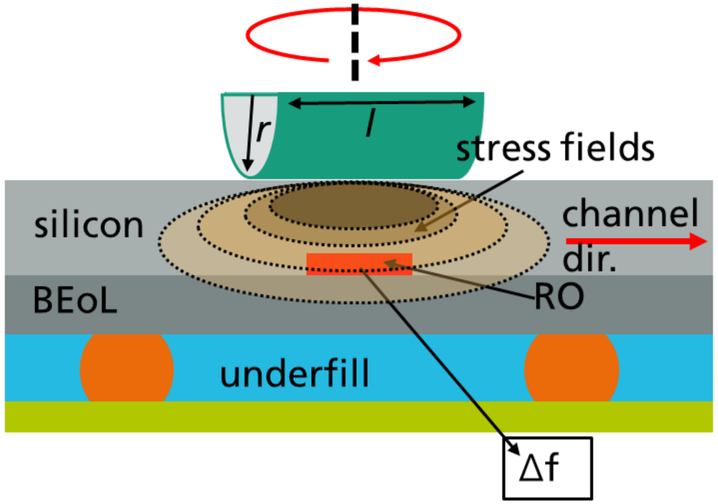
- **Almost biaxial tensile stress**
- Shear stress negligible

Relevant parameters influencing the indentation experimental approach

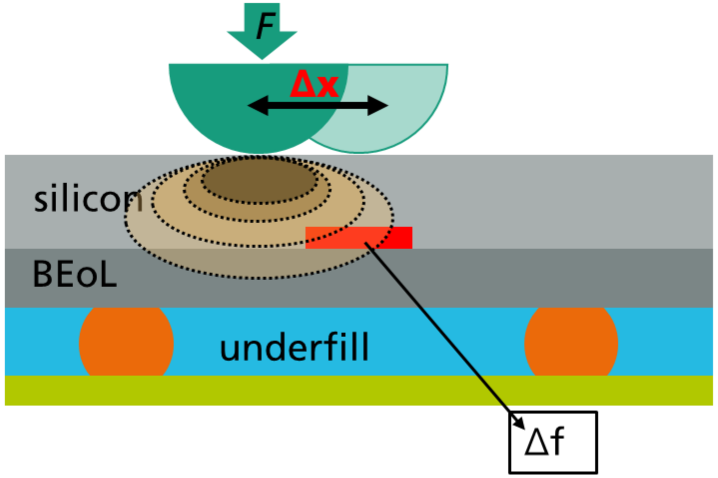
1) Silicon thickness



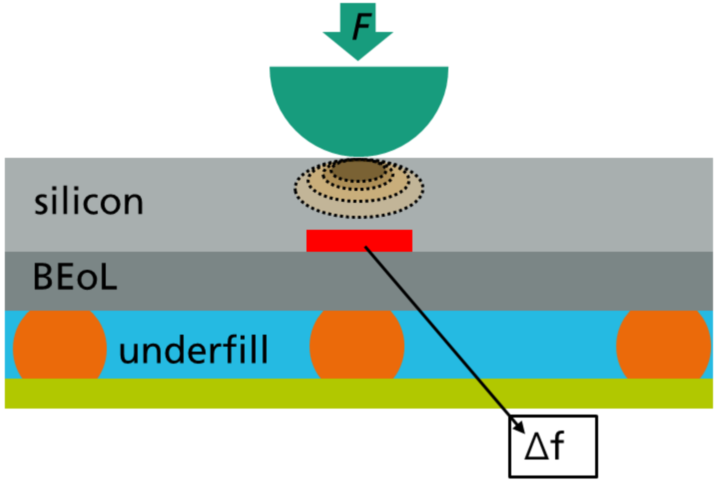
2) Tip geometry



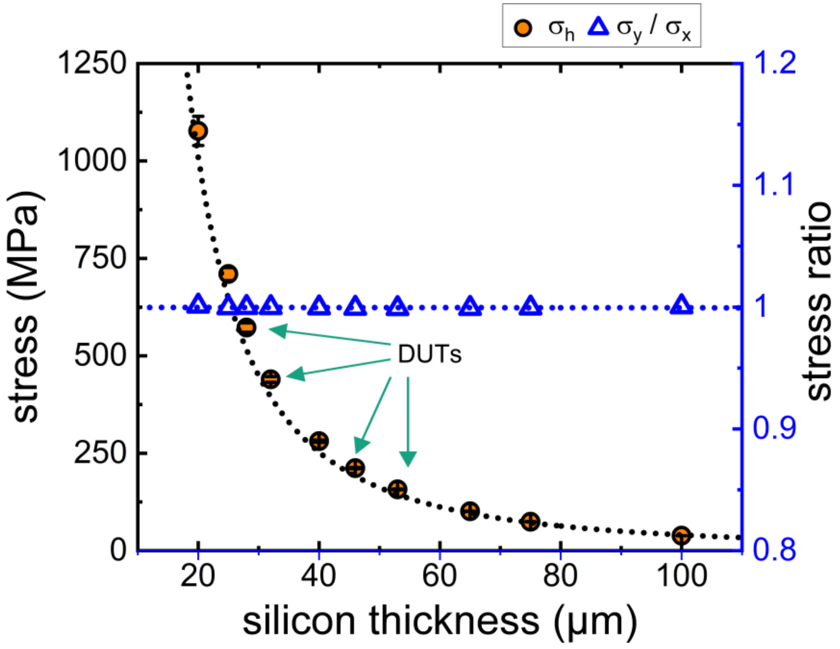
3) Tip offset

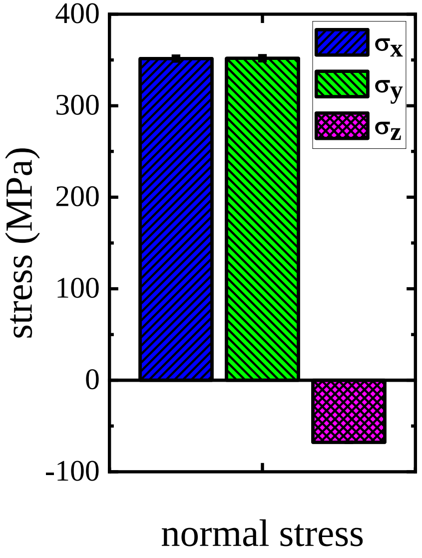


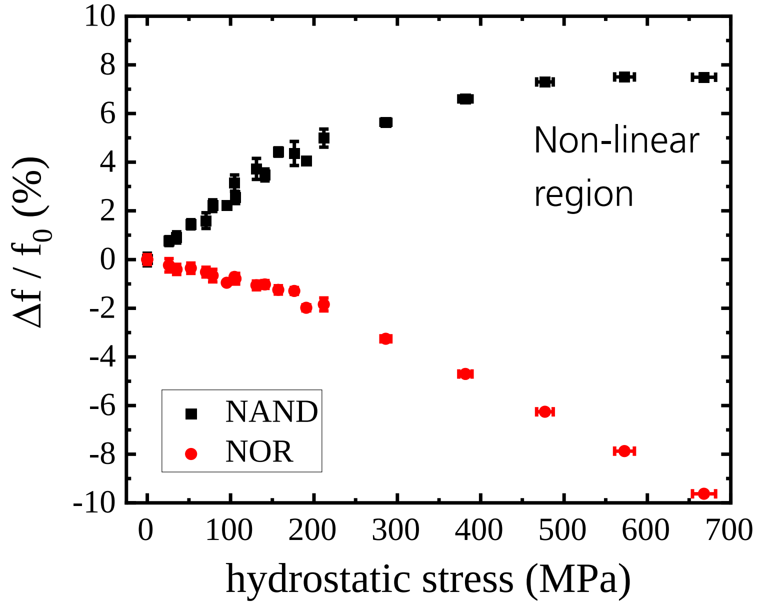
4) Chip layout



Influence of Silicon thickness – spherical tips







FEM-simulation (1.2 N):

- Thickness dependent stress
- In-plane ratio constant

Dir. of strain change	**CMOS Performance**	
	NMOS	PMOS
x	++	--
y	+	+
z	-	+

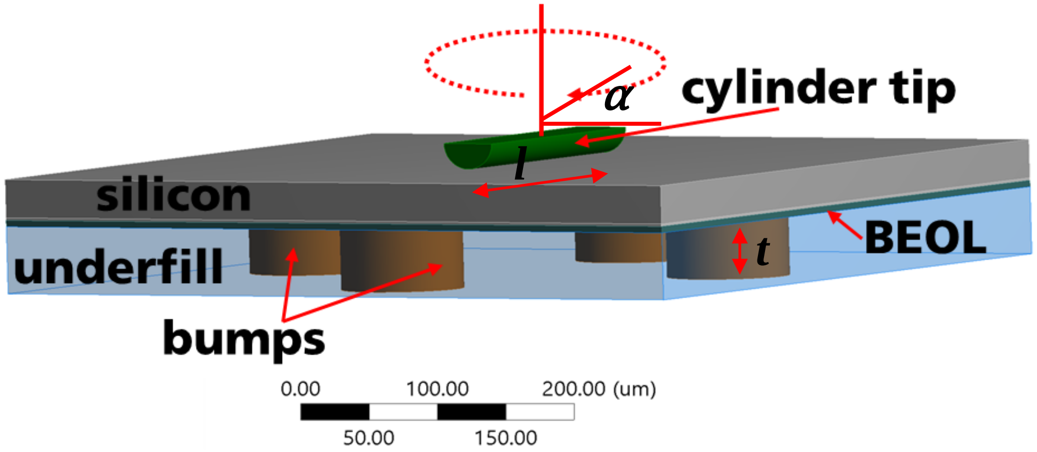
Experiment:

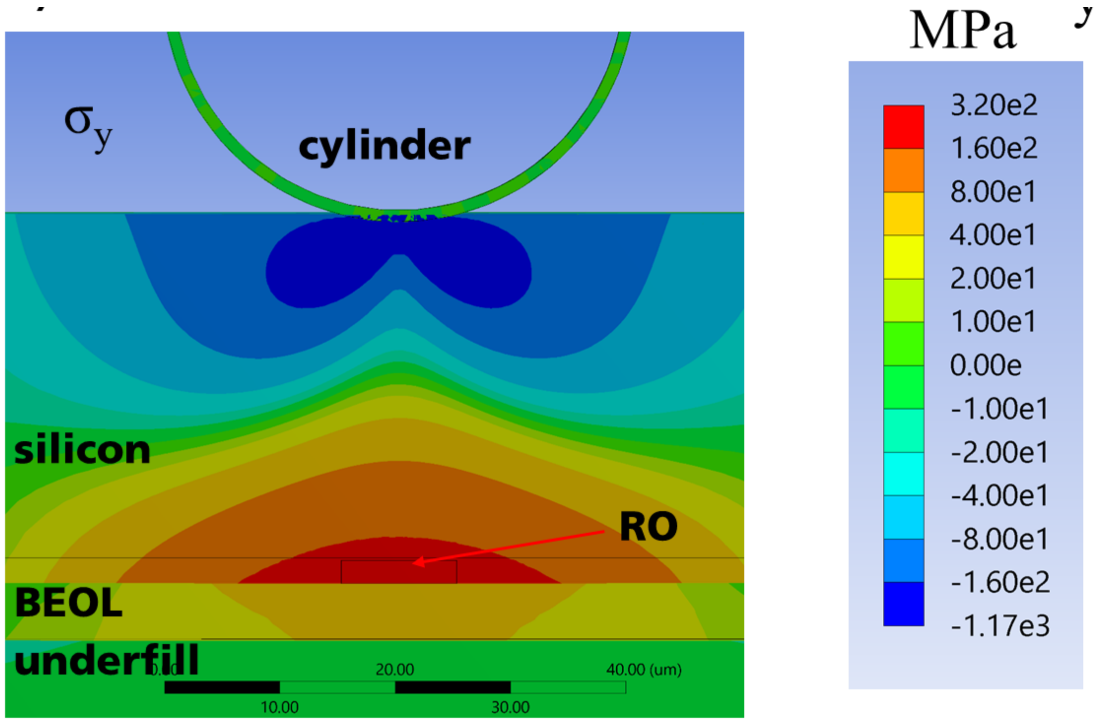
- Consistent data sets
- RO shifts for low and high stress

S. Schlipf et al., "Stress-induced transistor degradation studied by an indentation approach," *IEEE Transactions on Device and Materials Reliability, 2021*

Influence of tip geometry: Cylinder indentation

FE simulation to determine optimized experimental properties





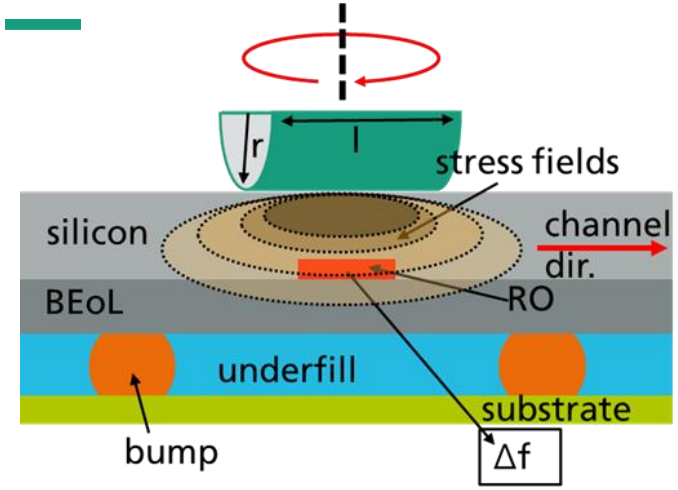
FE – geometry

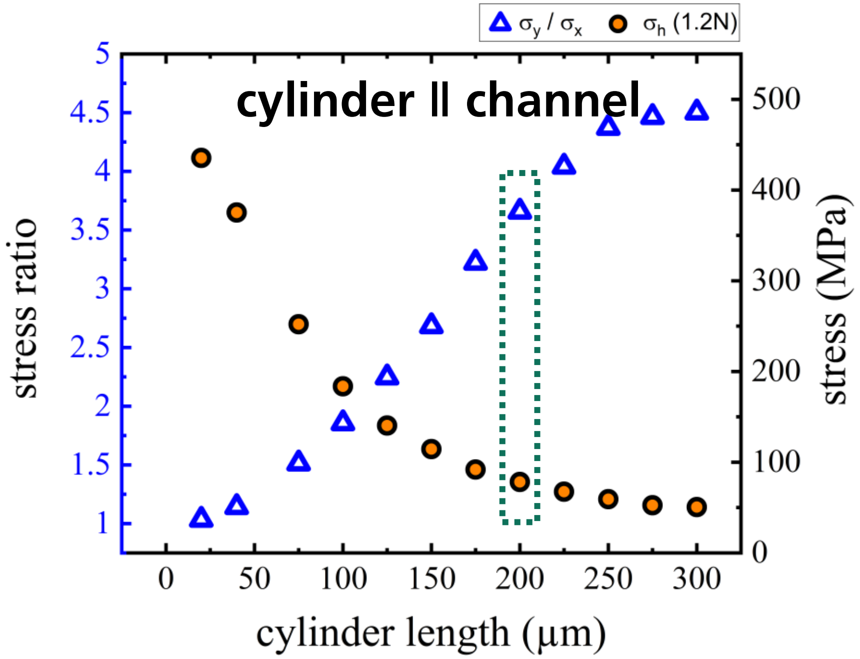
- Representative geometry including relevant layers in close distance to the contact

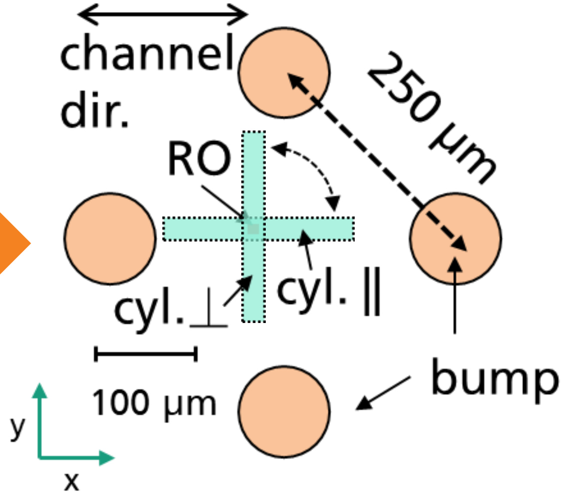
FE – results

- **Selective tensile in-plane stress at transistor region**

Influence of tip geometry: Cylinder indentation







Cylinder tips

- Control over stress fields
- Tip orientation relative to channel direction

FE-simulation

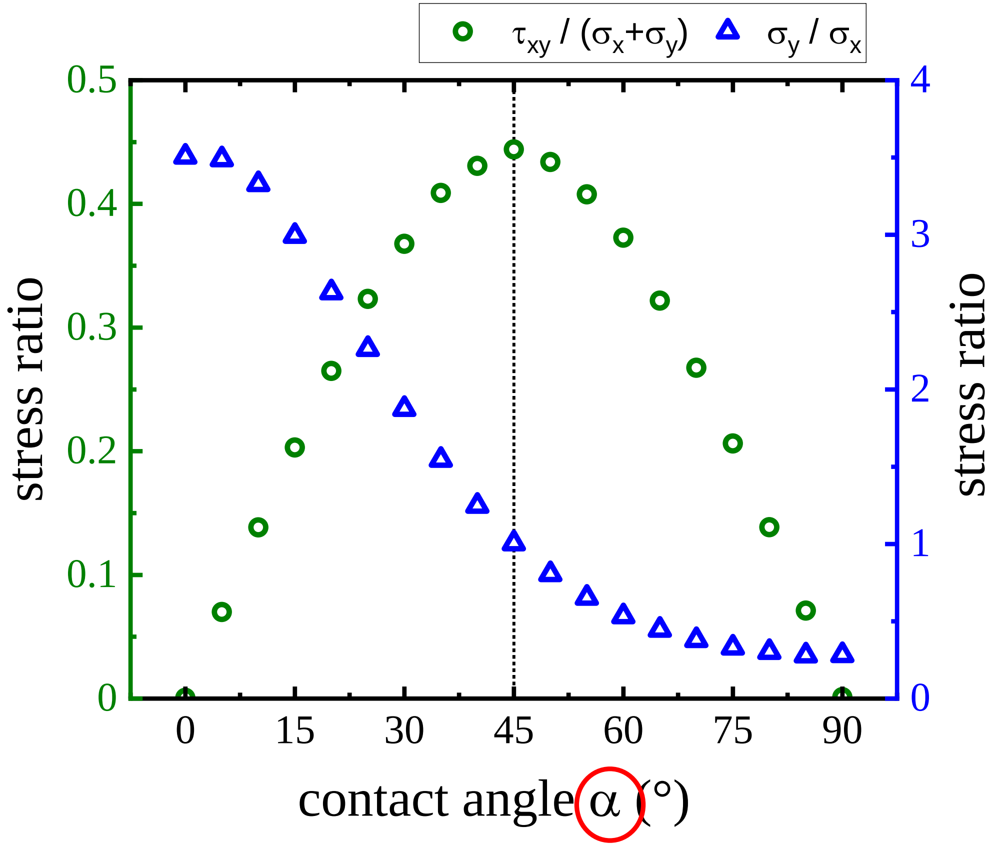
- Optimized tip properties (length)
- Stress fields with a dominating component

Chip - layout

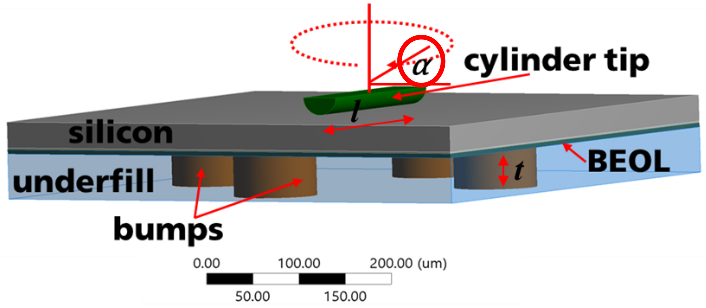
- Setup closely related to three-point bending

S. Schlipf et al., "Piezoresistive Characteristics of MOSFET Channels Determined With Indentation," *IEEE Transactions on Electron Devices, 2021*

Influence of tip geometry: Cylinder indentation contact angle



In-plane - and shear - vs. normal stress ratio as a function of the contact angle



Parameters:

Cylinder length l = 200 µm

Silicon thickness t = 32 µm

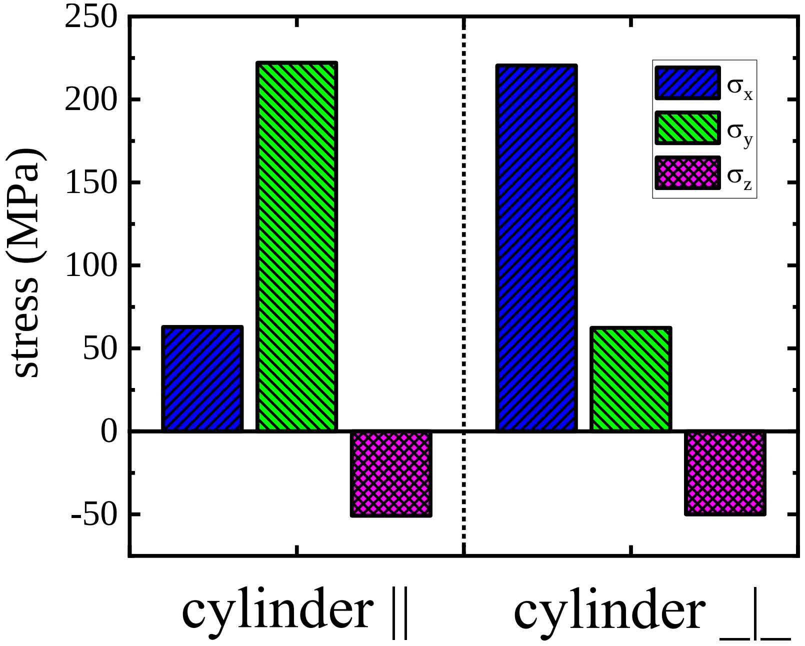
Results:

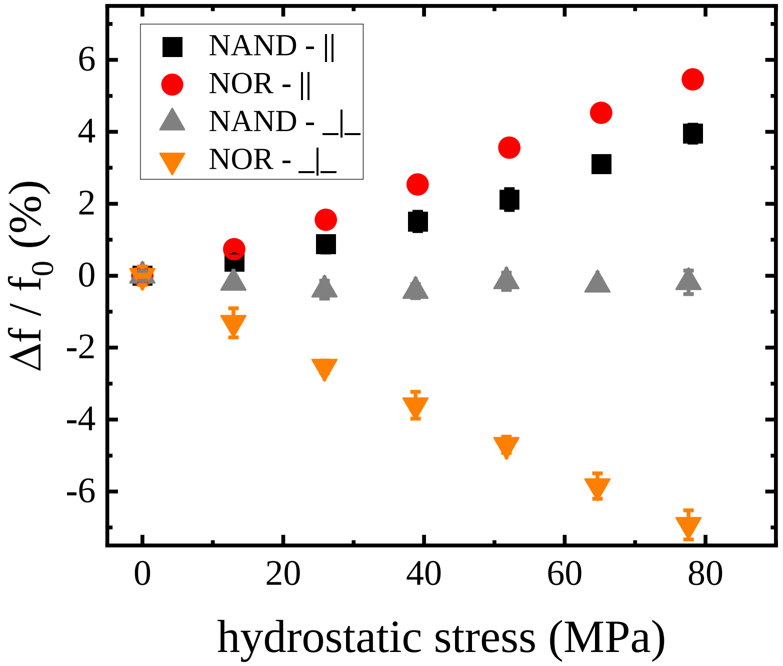
In-plane stress ratio is transformed from σ_y- to σ_x-component

Clear shear stress maximum for a contact angle of 45° (and biaxial in-plane components)

Presented at IEEE IIRW 2021: Schlipf et al. : “Shear stress effects on the device characteristics determined with indentation testing”

Cylinder indentation – FEM and experimental data





FE-simulation

- Tip orientation dependent stress fields
- Strongly dominating stress component

Experiment

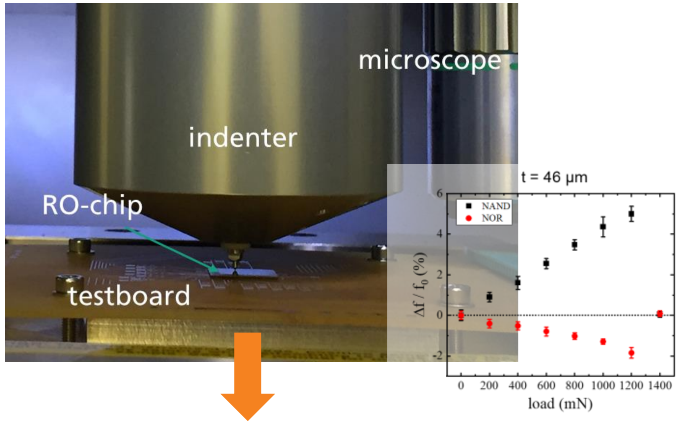
- Tip orientation dependent signal shifts

→ Frequency shifts correlate with stress fields

S. Schlipf et al., "Nanoindentation to investigate IC stability using ring oscillator circuits as a CPI sensor," *in 2020 IEEE IRPS*

Deriving directional stress effects with indentation data

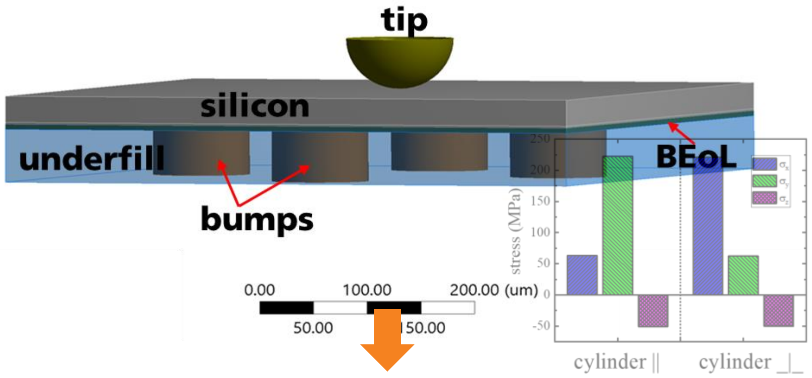
1) Electrical – mechanical study



Electrical shifts: (Δf_1) (Δf_2) (Δf_3)

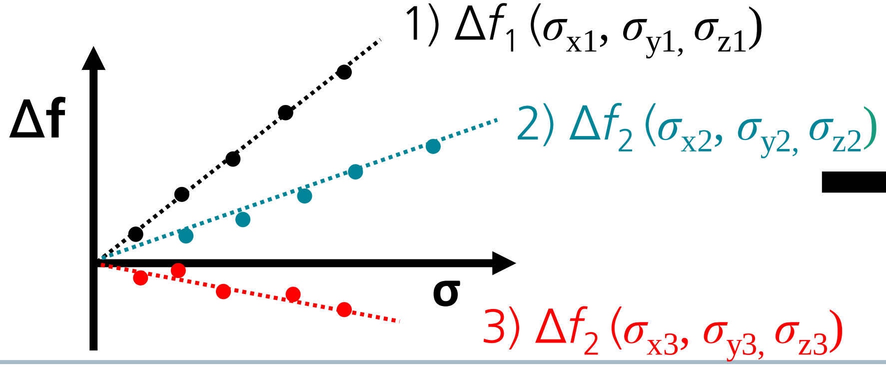
Layout, materials, contact force …

2) FE-study



Stress tensor: $(\sigma_{x1}, \sigma_{y1}, \sigma_{z1})$
$(\sigma_{x2}, \sigma_{y2}, \sigma_{z2})$
$(\sigma_{x3}, \sigma_{y3}, \sigma_{z3})$

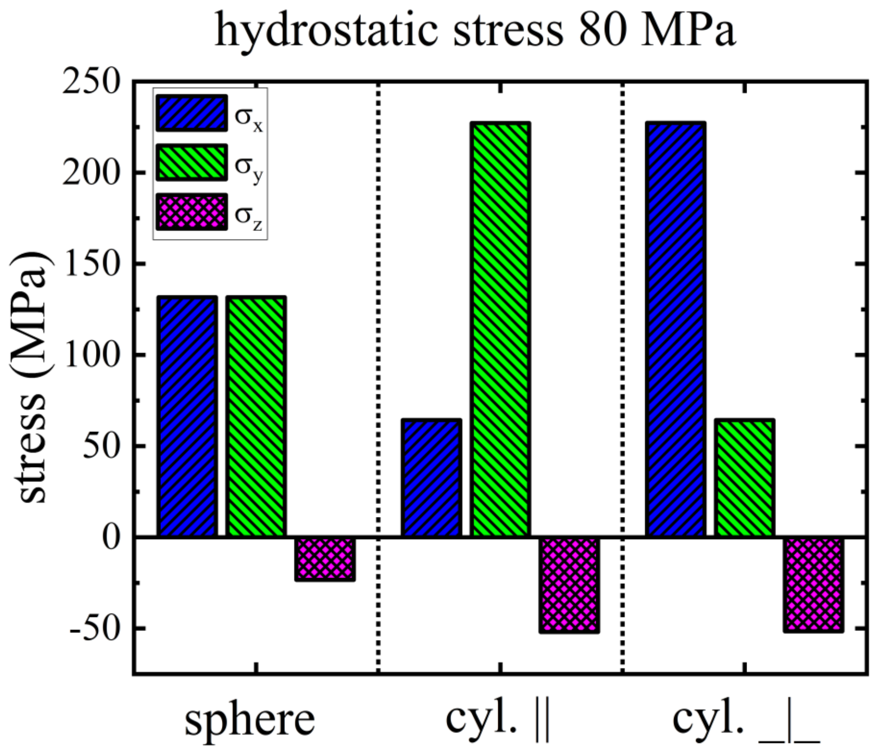
3) Combining experiments

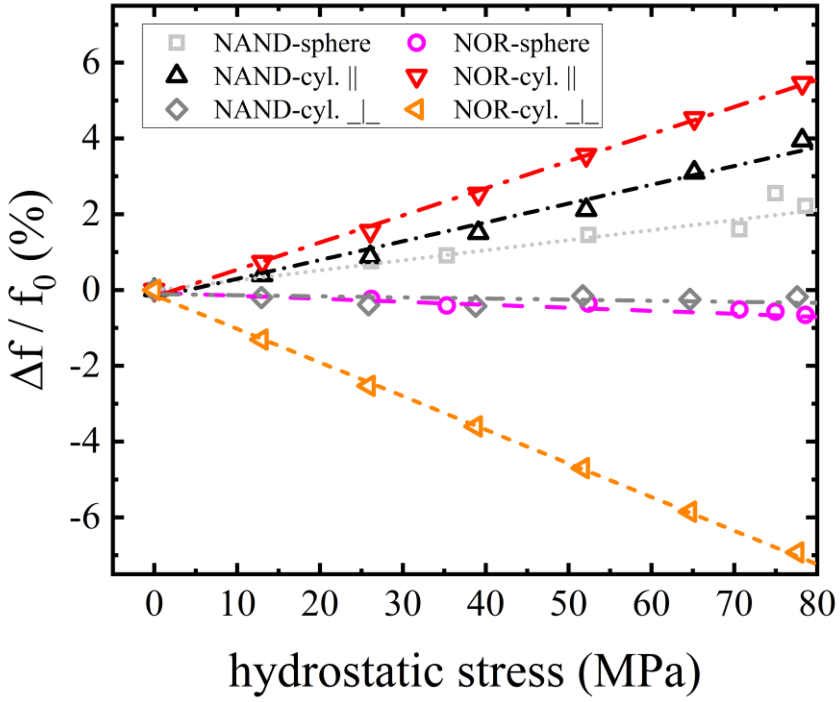


$$\frac{\Delta\mu}{\mu_0} = \sigma_x \pi_x + \sigma_y \pi_y + \sigma_z \pi_z$$

$$\begin{pmatrix} \sigma_{x1} & \sigma_{y1} & \sigma_{z1} \\ \sigma_{x2} & \sigma_{y2} & \sigma_{z2} \\ \sigma_{x3} & \sigma_{y3} & \sigma_{z3} \end{pmatrix} \begin{pmatrix} \pi_x \\ \pi_y \\ \pi_z \end{pmatrix} = \begin{pmatrix} \Delta f_1 \\ \Delta f_2 \\ \Delta f_3 \end{pmatrix}$$

FEM and experimental data of three indentation experiments





<u>FE-simulation</u>

- Tip geometry related stress fields
- Three linear independent experiments

<u>Experiment</u>

- RO data for all three tip geometries
- **Linear fitting** → specific sensitivity

S. Schlipf et al., “Piezoresistive Characteristics of MOSFET Channels Determined With Indentation,” *IEEE Transactions on Electron Devices, 2021*

Piezoresistive coefficients obtained from indentation

$$\begin{array}{cccccc} \left(\begin{array}{cccccc} a*\sigma_x & a*\sigma_y & a*\sigma_z & b*\sigma_x & b*\sigma_y & b*\sigma_z \\ b*\sigma_x & b*\sigma_y & b*\sigma_z & a*\sigma_x & a*\sigma_y & a*\sigma_z \\ a*\sigma_x & a*\sigma_y & a*\sigma_z & b*\sigma_x & b*\sigma_y & b*\sigma_z \\ b*\sigma_x & b*\sigma_y & b*\sigma_z & a*\sigma_x & a*\sigma_y & a*\sigma_z \\ a*\sigma_x & a*\sigma_y & a*\sigma_z & b*\sigma_x & b*\sigma_y & b*\sigma_z \\ b*\sigma_x & b*\sigma_y & b*\sigma_z & a*\sigma_x & a*\sigma_y & a*\sigma_z \end{array}\right) & \begin{pmatrix} \pi_{x-N} \\ \pi_{y-N} \\ \pi_{z-N} \\ \pi_{x-P} \\ \pi_{y-P} \\ \pi_{z-P} \end{pmatrix} & = & \begin{pmatrix} \Delta F_{NAND1} \\ \Delta F_{NOR1} \\ \Delta F_{NAND2} \\ \Delta F_{NOR2} \\ \Delta F_{NAND3} \\ \Delta F_{NOR3} \end{pmatrix} \\ \underbrace{\hphantom{a*\sigma_x \quad a*\sigma_y \quad a*\sigma_z}}_{\text{NMOS}} \underbrace{\hphantom{b*\sigma_x \quad b*\sigma_y \quad b*\sigma_z}}_{\text{PMOS}} & & & \end{array}$$

	Experiment FDSOI		Literature bulk[2]	
	NMOS	**PMOS**	NMOS	PMOS
	[10^{-11} Pa^{-1}]			
π_x	**-35.2±2.5**	**79.4±2.5**	-35.5	71.7
π_y	**-8.5±2.5**	**-37.7±2.5**	-14.5	-33.8
π_z	**37±37**	**-17±37**	27.0	-20.0

- Linear system
  - Linearized piezoresistive model[1]
  - Stress (σ_x , σ_y , σ_z)
  - Transistor ratio in the gates (a = 2/3; b = 1/3)
  - ΔF_{NAND} , ΔF_{NOR}

- Computed coefficients
  - In-plane components in good agreement with literature
  - Out-of-plane less defined

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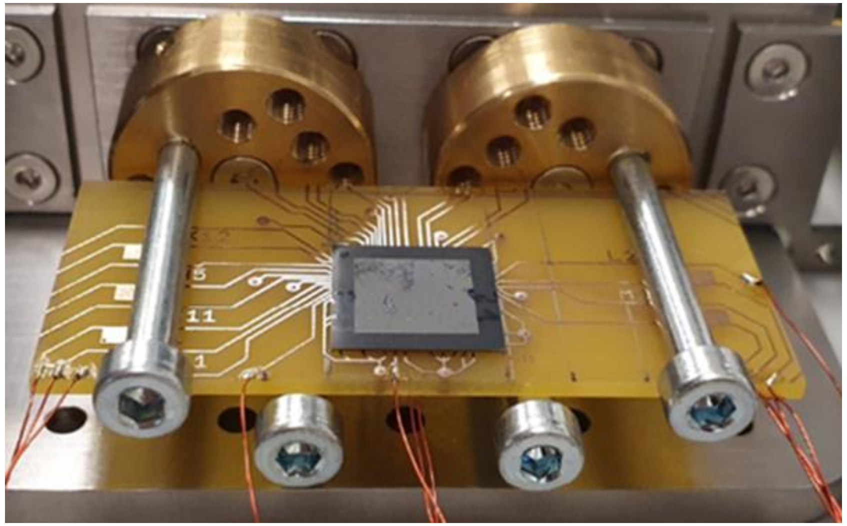
[1] Thompson et al., "*Uniaxial-process-induced strained-Si: extending the CMOS roadmap*"

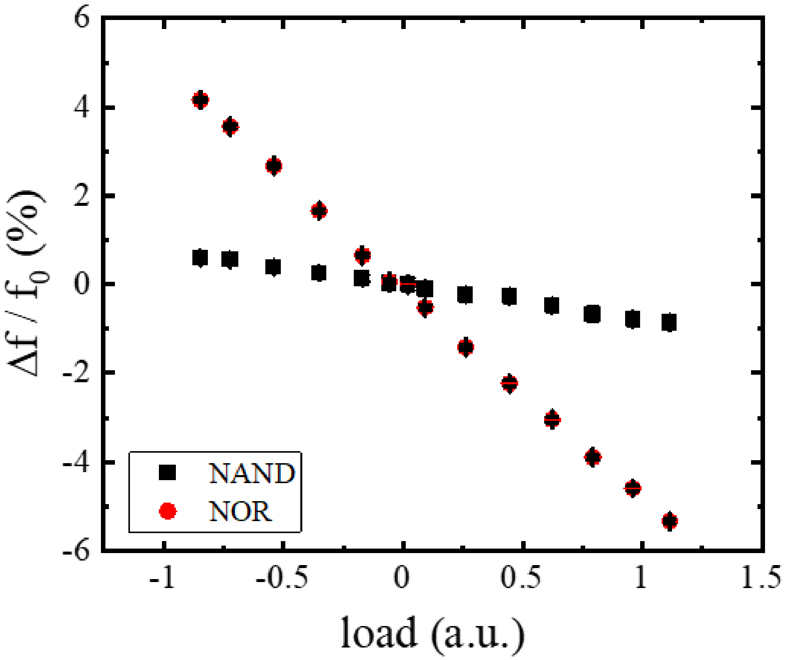
[2] Thompson et al., "*Future of Strained Si/Semiconductors in Nanoscale MOSFETs*"

Validation using Four – point bending



<u>Rotational bending experiments</u>

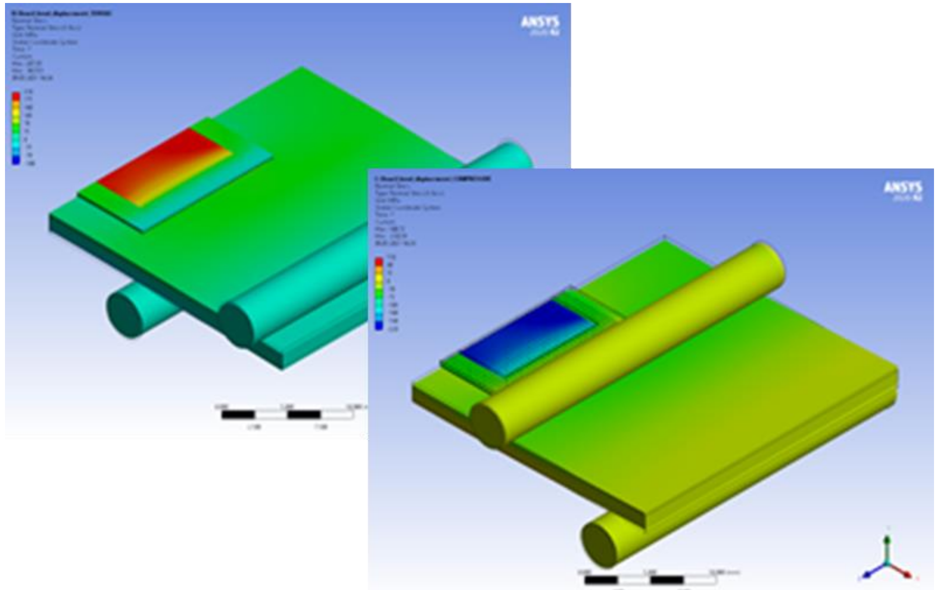
- Tensile and compressive stress
- Influence of board warpage on device characteristics



- Bending parallel to the transistor channels (x)
- Strong shift of NOR circuit due to degradation of the PMOS devices

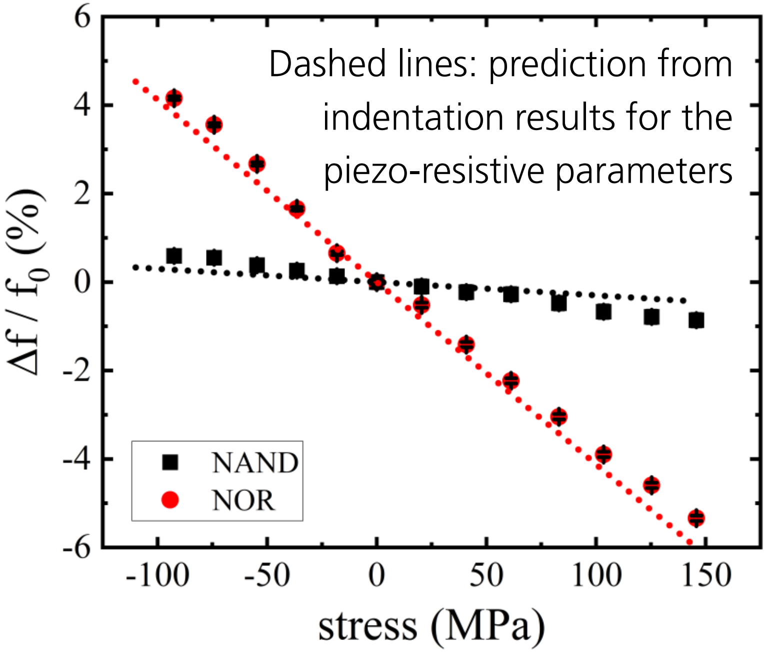
Presented at EuroSimE 2021: Schlipf et al. : "*IC package related stress effects on the characteristics of ring oscillator circuits*"

Validation using Four – point bending



FE simulation

- Stress in the Chip, package, board
- Critical stress at solder joints
- Stress at RO location

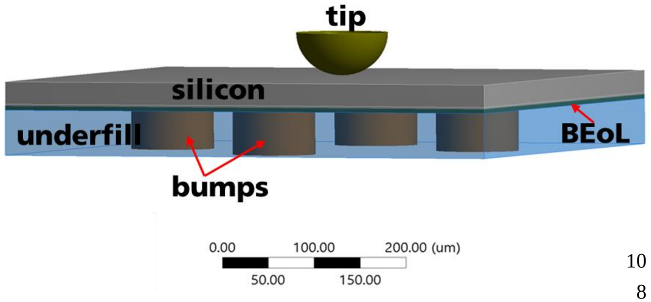


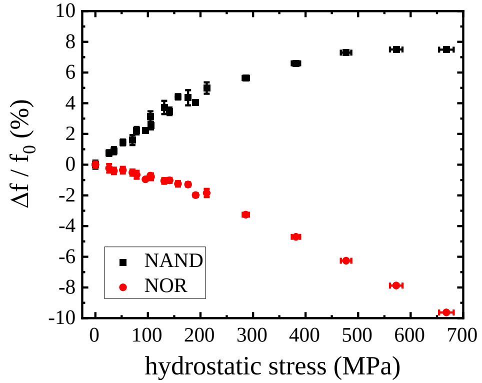
- RO signal shifts vs. stress with predicted values from indentation
- Validation π-coefficients from indentation[1]
- confirms indentation as a reliable technique to study stress effects

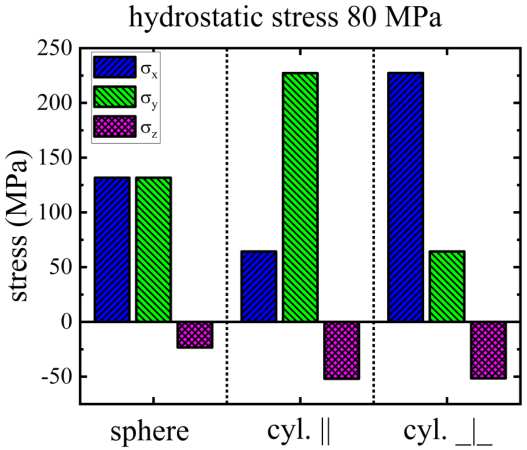
Schlipf et al. : "*Piezoresistive Characteristics of MOSFET Channels Determined With Indentation*" IEEE TED 2021

Summary

- Methodology based on indentation to study stress effects in MOSFETs
- Explainable RO behavior and consistent RO frequency shifts vs. stress correlations
- Controlling the stress fields with optimized tip geometries (FEM) to generate stress conditions closer to biaxial / uniaxial stress
- Combining the experimental data and FE simulation of three independent indentation experiments to determine the piezoresistive coefficients







$$\left(\underbrace{\begin{matrix} a*\sigma_x & a*\sigma_y & a*\sigma_z \\ b*\sigma_x & b*\sigma_y & b*\sigma_z \\ a*\sigma_x & a*\sigma_y & a*\sigma_z \\ b*\sigma_x & b*\sigma_y & b*\sigma_z \\ a*\sigma_x & a*\sigma_y & a*\sigma_z \\ b*\sigma_x & b*\sigma_y & b*\sigma_z \end{matrix}}_{\text{NMOS}} \underbrace{\begin{matrix} b*\sigma_x & b*\sigma_y & b*\sigma_z \\ a*\sigma_x & a*\sigma_y & a*\sigma_z \\ b*\sigma_x & b*\sigma_y & b*\sigma_z \\ a*\sigma_x & a*\sigma_y & a*\sigma_z \\ b*\sigma_x & b*\sigma_y & b*\sigma_z \\ a*\sigma_x & a*\sigma_y & a*\sigma_z \end{matrix}}_{\text{PMOS}}\right) \begin{pmatrix} \pi_{x-N} \\ \pi_{y-N} \\ \pi_{z-N} \\ \pi_{x-P} \\ \pi_{y-P} \\ \pi_{z-P} \end{pmatrix} = \begin{pmatrix} \Delta F_{NAND1} \\ \Delta F_{NOR1} \\ \Delta F_{NAND2} \\ \Delta F_{NOR2} \\ \Delta F_{NAND3} \\ \Delta F_{NOR3} \end{pmatrix}$$

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Projects „RingO“ and „RingO 2“ (GLOBALFOUNDRIES and FH IKTS in the frame of IPCEI for ME)

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Schlipf et al., IEEE Transactions on Electron Devices 2021, vol. 68, no. 4.

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Vielen Dank für Ihre Aufmerksamkeit

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Outlook

- Piezoresistive characteristics of different technologies (confinement in FinFET architectures[1])
- Combination of micromechanical loading experiments and electrical device behavior (Cu Pillar loading[2]…)
- Directional stress effects on transistor degradation mechanisms[3] (trapping, NBTI)
- Usage of the calibrated RO structures as a CPI stress sensor

[1] Chu et al., "Strain: A Solution for Higher Carrier Mobility in Nanoscale MOSFETs"
[2] Geisler et al., "CPI assessment using a novel characterization technique based on bump-assisted scratch-indentation testing"
[3] Kruv et al. , "On the impact of mechanical stress on gate oxide trapping"