17th International Conference Reliability and Stress-Related Phenomena in Nanoelectronics

„Stress workshop“

Abstract booklet

April, 24 – April, 26, 2023

Bad Schandau, Germany

Sponsors:

17th International Conference Reliability and Stress-Related Phenomena in Nanoelectronics

Scope

More than ever before, materials-driven product innovations in semiconductor industry and shorter time-to-market introductions for new micro- and nanoelectronic products require high advancement rates and tight coupling between research, development and manufacturing. Since novel product design and process steps, and particularly the integration of new materials, require the understanding of stress-related phenomena to ensure the requested product lifetime, reliability physics and engineering as well as materials engineering and nano-scale materials characterization are considered as fundamental drivers for innovation in semiconductor industry.

Traditionally, this series of conferences has been focused on stress arising in micro- and nano-scale structures of on-chip interconnect stacks and advanced packaging structures. This thermomechanical stress can lead to degradation phenomena such as crack propagation caused by chip-package interaction and to the acceleration of known reliability-limiting processes in backend-of-line stacks such as electromigration and time-dependent dielectric breakdown. The 17th conference will include two new focus areas:

- Reliability at harsh environments (e.g. space, automotive),
- Materials behavior and reliability of organic and flexible electronics

The conference will cover the whole range from fundamental research to industrial applications. It will provide a forum for scientists and engineers from universities, research institutions and industry to discuss current challenges and future scenarios related to reliability and stress-induced phenomena in micro- and nanoelectronics.

Co-Chairs:

- Ehrenfried Zschech, deepXscan Dresden & Technische Universität Dresden, Germany
- Reiner Dauskardt, Stanford University, Palo Alto/CA, USA
- Valeriy Sukharev, Mentor Graphics / Siemens EDA, Fremont/CA, USA
- Olivier Thomas, Aix-Marseille Universite, France
- Zhong Chen, NTU Singapore

Venue:

Hotel Elbresidenz Bad Schandau near Dresden, Germany

Organizational committee

Dominik Gronarz, Organic Electronics Saxony, Dresden, Germany
Kristina Kutukova, deepXscan GmbH, Dresden, Germany
Johann Zeller, student, Dresden, Germany
Kim Brendel, Hotel Elbresidenz, Bad Schandau, Germany

Contact / Help:

Kristina Kutukova
Mobile phone: +491733969207

Symposium management
Organic Electronics Saxony Cluster

Topics of the conference

- Stress-related issues for advanced nonvolatile memories, including embedded phase-change memory
- Materials behavior at low temperatures for quantum computing, reliabilty-related aspects
- Scaling limitations of materials
- Role of microstructure and interfaces on mechanical behaviour of nanostructures
- Stress and thermal effects in advanced packaging, heterogeneous integration, and chip-package interaction
- Thermo-mechanical properties and stress: Measurements and simulation
- Advanced characterization techniques
- Compact modeling and statistical methods in circuit/device life-time assessment
- Thermal and stress-driven floor-planning methodology, stress mitigation techniques, and design technology co-optimization
- Reliability physics and engineering, damage and failure mechanisms
- Stability and lifetime of organic and flexible electronics
- Lifetime and ageing of nanoscale materials, structures and systems at low and high temperatures
- Component (device / interconnect) reliability vs. system reliability
- Reliability of products at harsh environments
- Reliability of power devices

Highlights

- Podium discussion „Reliability of automotive electronics“ with Andreas Aal (VOLKSWAGEN) and Oliver Aubel (GLOBALFOUNDRIES)
- Hiking tour in Saxonian Switzerland
- 2 Poser sessions and 3 best poster awards
- Conference dinner
- Lab tour at deepXscan

Session Chairs:

- Ehrenfried Zschech, deepXscan Dresden & Technische Universität Dresden, Germany
- Carl V. Thompson, MIT, Boston/NY, USA
- Reiner Dauskardt, Stanford University, Palo Alto/CA, USA
- Christoph Gammer, ESI Leoben, Austria
- Rodrigo Martins, Uninova Lisabon, Portugal
- André Clausner, Fraunhofer IKTS Dresden, Germany
- Olivier Thomas, Aix-Marseille Universite, France
- Kristina Kutukova, deepXscan Dresden, Germany

Scientific Committee:

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- Natalia Sobczak, IMIM PAN Cracow, Poland
- Oden Warren, Bruker, Minneapolis/MN, USA
- Ingrid de Wolf, IMEC Leuven, Belgium
- Xiaopeng Xu, Synopsys, Mountain View/CA, USA

Invited Speakers:

- André Clausner, Fraunhofer IKTS Dresden, Germany
- Carl V. Thompson, MIT, Boston/NY, USA
- Christoph Gammer, ESI Leoben, Austria
- Daniel Nemecek, TESCAN Brno, Czech Republic
- Ehrenfried Zschech, deepXscan Dresden, Germany
- Hiroshi Nishikawa, Osaka University, Japan
- Ingrid de Wolf, IMEC Leuven, Belgium
- Iuliana Panchenko, Technische Universität Dresden, Germany
- Jörg Acker, Brandenburg University of Technology Cottbus-Senftenberg, Germany
- Karl Leo, Technische Universität Dresden, Germany
- Kristina Kutukova, deepXscan Dresden, Germany
- Lionel Vignoud, CEA-LETI Grenoble, France
- Matthias Stecher, Infineon Technologies, Munich, Germany
- Olivier Thomas, Aix Marseille Universitem Marseille, France
- Pal-Jen Wei, Bruker, Taiwan
- Reinhold Dauskardt, Stanford University Palo Alto/CA, USA
- Robert Filipek, AGH Krakow, Poland
- Rodrigo Martins, Uninova Lisabon, Portugal
- Sandrine Lhostis, ST Microelectronics Crolles, France
- Susann Rothe, Technical University Dresden, Germany
- Vikas Tapan, Siemens, Munich, Germany
- Wiebke Langgemach, Fraunhofer FEP, Dresden, Germany

Program

Monday 24th April 2023

		Chair: Ehrenfried Zschech	Session 1: Reliability in micro- and nanoelectronics
	08:45	Ehrenfried Zschech deepXscan, Dresden, Germany	*Opening remarks*
T1	09:00	Sandrine Lhostis STMicroelectronics, France	*New reliability challenges for 3D integration stacking using hybrid bonding*
T2	09:30	Susann Rothe Technical University Dresden, Germany	*Combined Modeling of Electromigration, Thermal and Stress Migration in AC Interconnect Lines*
T3	10:00	Ingrid de Wolf, Vladimir Chairman IMEC, Leuven, Belgium	*FinFETs: Sensing and feeling mechanical stress*
10:30 – 11:00		**Break**	
		Chair: Carl V. Thompson	**Session 2: Impact of stress on device properties**
T4	11:00	Kristina Kutukova deepXscan, Dresden, Germany	*In-situ nano-XCT study of the local energy release rate for crack propagation in advanced ICs*
T5	11:30	Pal Jen Wie Bruker, Taiwan	*Indentation-Induced Delamination and Adhesion Work Evaluation at Elevated Temperature in Semicon Industrial Cases*
T6	12:00	André Clausner Fraunhofer IKTS, Dresden, Germany	*Studying stress effects in transistor channels by nanoindentation with varied contact geometries*
T7	12:30	Reinhold Dauskardt Stanford University, Palo Alto/CA, USA	*Hybrid Dielectric Films for Device Technologies: Understanding Relationships between Molecular Structure, Processing and Function*
13:00 – 14:30		**Lunch Break**	
		Chair: Reinhold Dauskardt	**Session 3: Robustness of engineered systems: From design to application**
T8	14:30	Vikas Tapan Siemens, Munich, Germany	*Early architectural exploration with PAVE360*
T9	15:00	Hiroshi Nishikawa Osaka University, Japan	*Solid-phase bonding process using nanostructured surface for power devices in automotive*
	15:30	**Chair: Kristina Kutukova**	***Poster Session***
	17:00	**Moderators:** • Andreas Aal, VOLKSWAGEN • Oliver Aubel, GLOBALFOUNDRIES **Key Contributors:** • Joe McPherson • Günter Haas (Entegris) • Tapan Vikas (SiemensEDA) • Nir Sever (proteanTecs)	***Podium discussion „Reliability of automotive electronics“*** Context: *Upcoming hardware challenges on the way towards the Software-defined-Vehicle*
19:00		**BBQ**	

Tuesday 25th April 2023

		Chair: Christoph Gammer	Session 4: Materials characterization for device development and reliability engineering
T10	09:00	Iuliana Panchenko Technical University Dresden, Germany	*Hybrid bond and nanowired bump technologies for high density interconnect formation on wafer level*
T11	09:30	Olivier Thomas, Aix Marseille University, France	*Phase change materials for embedded memories: in situ investigation of crystalli-zation behavior using synchrotron radiation*
T12	10:00	Ehrenfried Zschech, deepXscan, Dresden, Germany	*Controlled microcrack steering into toughened regions – What microelectronics can learn from nature?*
10:30 – 11:00		**Break**	
		Chair: Rodrigo Martins	**Session 5: Degradation mechanisms and materials behaviour**
T13	11:00	Matthias Stecher Infineon Technologies, Munich, Germany	*Degradation mechanisms of 10kV-reinforced isolated gate drivers at high switching frequencies greater than 30kHz*
T14	11:30	Carl V. Thompson MIT, Boston/NY, USA	*Contrasting Stress Evolution During Lithiation and Delithiation of Different Electrode Materials for Thin Film Batteries*
T15	12:00	Robert Filipek AGH Krakow, Poland	*Tortuosity and Porosity in Electrochemical Systems – Computed Tomography Based 3D Transport Modelling*
T16	12:30	Jörg Acker Brandenburg University of Technology Cottbus-Senftenberg, Germany	*Reliability and Recycling of Battery Materials*

13:00 – 14:00	**Lunch Break**	
14:00	***Hiking tour in Saxonian Switzerland***	
17:30	**Chair: Kristina Kutukova**	***Poster session***
20:00	**Conference Dinner**	

Wednesday 26th April 2023

		Chair: André Clausner	**Session 6: Micro- and nanomechanics**
T17	09:00	Lionel Vignoud CEA-LETI, Grenoble, France	*Strains and stresses control in microelectronic devices: How to optimize the steps from design to manufacturing?*
T18	09:30	Daniel Nemecek TESCAN, Brno, Czech Republic	*Advancing nanoscale characterization of semiconductor devices by effortless 4D-STEM workflows*
T19	10:00	Christoph Gammer, ESI Leoben, Austria	*Recent advances in nanoscale strain mapping using 4D STEM*
10:30 – 11:00		**Break**	
		Chair: Olivier Thomas	**Session 7: Reliability of organic electronics**
T20	11:00	Rodrigo Martins Uninova Lisbon, Portugal	*Eco-Strategies for next generation electronics*
T21	11:30	Wiebke Langgemach Fraunhofer FEP, Dresden, Germany	*Processing flexible glass – thin film stress and its influence on glass durability*
T22	12:00	Karl Leo Technical University Dresden, Germany	*Organic semiconductors – from a lab curiosity to serious applications*
	12:30	Ehrenfried Zschech deepXscan, Dresden, Germany	*Closing remarks*
13:00 – 14:00		**Lunch Break**	

Poster session

Monday, 24th April 2023 15:30 and Tuesday, 25th April 2023 17:30

Poster	Author	Title
P1	Susann Rothe	*A Proactive Design Approach to Avoid Migration-Induced Failure in IC Interconnects*
P2	Verena Hein	*The Influence of the Interconnect Material on the Performance of a Highly Robust Metallization Layout*
P3	Stefan Weitz	*Micromechanical in-situ studies of on-chip interconnect stack structures using X-ray microscopy*
P4	Michael Reisinger	*Characterization of the thermo-mechanical behavior of Cu metallization in microelectronic applications*
P5	Tobias Ziegelwanger	*Local gradients of microstructure and residual stresses in Si device sidewalls separated by laser dicing*
P6	André Lange	*Investigating HCI and BTI degradation in 4H-SiC CMOS*
P7	Jolanta Janczak-Rusch	*Nanomultilayers for thermal management and micro-/nano-joining*
P8	Bastian Rheingans	*Thin-film transfer by nanopaste sinter-bonding*
P9	Bowen Zhang	*In-situ TEM study and nanomechanical characterization of fracture behavior in two-dimensional covalent organic frameworks*
P10	Thomas Langner/Jörg Acker	*Shaping the topography of solar wafers due to increased reactivity of lattice strained silicon*
P11	Thomas Langner/Jörg Acker	*Deposition of copper in lithium-ion batteries during the deep discharge process*
P12	Thomas Langner/Jörg Acker	*Degradation of Cathode Foils from Lithium-Ion Batteries in Humid Atmosphere*

Invited Talks and Posters

Contents

Invited talks:

Posters:

Abstracts
-Invited Talks-

New reliability challenges for 3D integration stacking using hybrid bonding

Sandrine Lhostis[1]*, Bassel Ayoub[1,2,3], Stéphane Moreau[3], Patrick Lamontagne[1], Hélène Frémont[2]

[1]STMicroelectronics: 850 rue Jean Monnet, F-38926 Crolles Cedex, France
[2]IMS Laboratory: University of Bordeaux, UMR 5218, 33405 Talence, France
[3]CEA-Leti: Univ. Grenoble Alpes, F-38000 Grenoble, France

**sandrine.lhostis@st.com*

Improving efficiency and performance is the main driver for microelectronic applications. The new trend named beyond Moore's law refers to the emergence of new architectures, processes, devices and materials [1]. 3D stacking is definitely an enabler for new architectures and packaging. During the last ten years, many demonstrations were done showing that stacking dies of different technologies enable new functionalities for optical sensor, memories and CPU devices [2-3]. Increasing the interconnect number by reducing the interconnection pitch between top and bottom tiers is key to get faster devices. Hybrid bonding, based on oxide-to-oxide and metal-to-metal direct bonding between the reported tiers, is a path for one of the most scalable integrations. We are interested here in the robustness of the hybrid bonding level when decreasing the interconnection pitch below submicrometric dimensions. The different features for reliability requirements are reviewed and discussed towards standard Back-End-Of-Line interconnects robustness.

Many integration flows have been developed for hybrid bonding stacking. The most critical integration scheme in terms of potential metal diffusion is based on a hybrid bonding interface made of silicon oxide and copper. We have developed a specific integration that is immune to copper diffusion into the faced oxide. This interface stability is assessed towards potential atomic and ionic diffusion [4]. The integrity of the hybrid bonding interface towards Cu diffusion is confirmed by dedicated Time Dependent Dielectric Breakdown studies through a novel test method. A different dependence between time-to-failure and electrical field is observed for the Cu/SiO_2 hybrid bonding configuration than for standard BEOL interconnects [5]. Another potential concern for a device is the repetitive thermomechanical stresses that could lead to interface delamination in the case of hybrid bonding integration. With pitch reduction, higher stress is expected at the bonding level due to the reduced spacing between the pads. This point is assessed by Thermal Cycling tests for pitch reduction [6]. Stress induced Voiding (SiV) may also be a concern. This failure mechanism is driven by the grain microstructure. In our developed integration, reducing the bonding pad size leads to the modification of the copper microstructure from polycrystalline to one-grain-dominant feature [7]. However, no modification of the robustness to SiV is identified even for bonding pad width reduced to 300nm [8]. Reliability under electron flow and thermal stress is performed through electromigration tests. Previous studies on large interconnect pitch have shown that the hybrid bonding level behaves as a standard BEOL level with failure occurring in the feeding lines. With sub-micron pad width reduction, a modification in the failure mechanism is identified. The extracted lifetime is still in line with the specifications [9].

In-depth studies on the Cu/SiO_2 hybrid bonding level indicate that this specific integration is robust to standard failure mechanisms for wafer -to-wafer interconnect pitch down to 710nm and pad width of 300 nm.

Acknowledgments
This work has received funding from the ECSEL Joint Undertaking (JU) under grant agreement No 826600 (project VIZTA). This work was also supported by the cooperative Research & Development program "IPCEI, Nano 2022 and by the French National Research Agency (ANR) under the "Investissements d'avenir" programs: ANR 10-AIRT-0005 (IRT NANO-ELEC).

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[3] S. Moreau et al., *ECS Journal of Solid State Science and Technology* **2022**, *11(2),* 024001.
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[9] S. Moreau et al., *IEEE International Reliability Physics Symposium (IRPS)* ***2023,*** to be presented

T2

Combined Modeling of Electromigration, Thermal and Stress Migration in AC Interconnect Lines

Susann Rothe*, Jens Lienig

Dresden University of Technology, Institute of Electromechanical and Electronic Design, 01062 Dresden, Germany, www.ifte.de

**susann.rothe@mailbox.tu-dresden.de*

The migration of atoms in metal interconnects in integrated circuits (ICs) increasingly endangers chip reliability. The susceptibility of DC interconnects to electromigration has been extensively studied. A few works on thermal migration and AC electromigration are also available. Yet, the combined effect of both on chip reliability has been neglected thus far.

This talk introduces both FEM and analytical models for atomic migration and steady-state stress profiles *in AC interconnects* considering electromigration, thermal and stress migration (EM, TM, and SM) *combined*. For this we expand existing models by the impact of self-healing, temperature-dependent resistivity, and short wire length. We conclude by analyzing the impact of thermal migration on interconnect robustness and show that it cannot be neglected any longer in migration-robustness verification.

Figure 1 illustrates our novel methodology which has been published in [1].

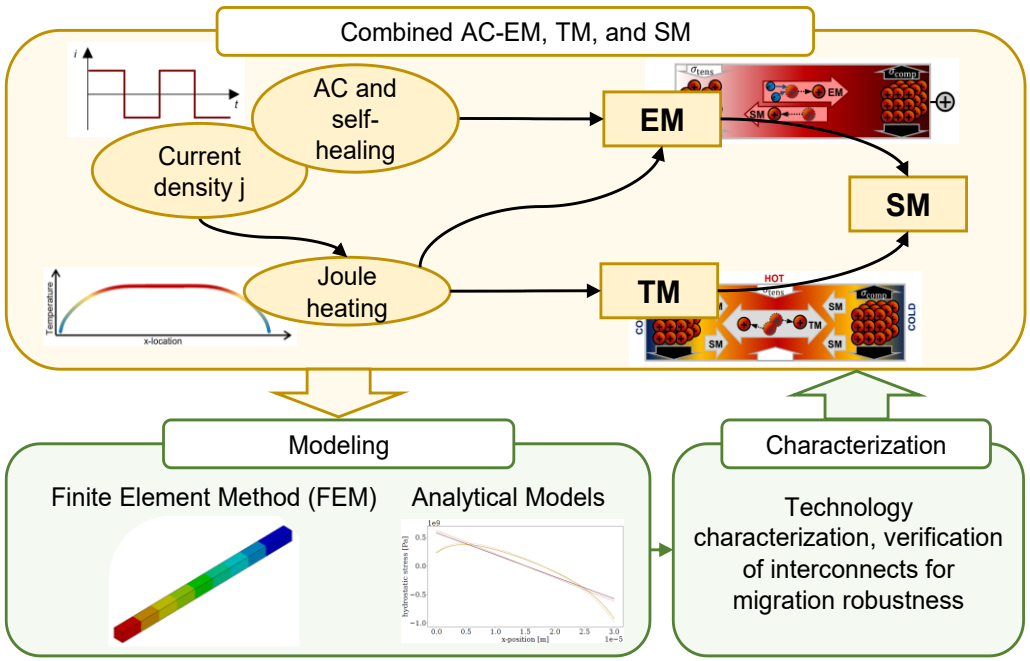

Figure 1. Illustration of the interactions of EM, TM, and SM (top) and the contribution of this talk (bottom). As shown on the lower left, we provide both FEM and analytical models which can be the basis for experimental technology characterization, migration robustness verification, and novel design strategies to mitigate migration-induced failures (lower right).

Reference

[1] S. Rothe, J. Lienig, "Combined Modeling of Electromigration, Thermal and Stress Migration in AC Interconnect Lines," *Proc. of the ACM 2023 Int. Symposium on Physical Design,* pp. 107–114, **2023**.

FinFETS: Sensing and feeling mechanical stress

Ingrid De Wolf[1,2]*, Vladimir Cherman[1]

[1]imec, Remiseboslaan 1, 3001 Leuven, Belgium
[2]Dept. Materials Science, Fac. Engineering Science, KU Leuven, Leuven, Belgium

**ingrid.dewolf@imec.be*

The impact of mechanical stress (MS) on mobility in Si and Ge, through the piezoresistivity effect, was already described in 1954 [1]. In 1991 first publications appeared discussing the impact of MS on MOSFET reliability [2,3]. MS was shown to affect hot-carrier degradation, which is directly related to its impact on mobility. With the advent of 3D-technology in the 21st century, there came an increasing concern that TSV-induced stress affects the nearby transistors, indicating the need for a 'keep-out zone' around the TSV, where no transistors should be placed [4,5]. Also chip-stacking and packaging induced mechanical stress effects on transistors raised concerns [6]. This was referred to as 'chip-package interaction (CPI)'. Over the years several researchers at imec studied the interaction between mechanical stress and FETs, either focusing on their sensitivity, or using them as sensors [3-8]. This talk presents an overview of the main results.

To study the impact of TSVs on FETs, dedicated test structures with transistors placed at different positions from the TSV were used. This allowed to determine the keep-out zone. It was found that the piezoresistive factors proposed by Smith [1] could not be used for these new technologies. It was also shown that stress-impact due to TSVs could be described using Lame's equation [5]. While for planar FETs n-type is less sensitive to mechanical stress than p-type, this is not the case for FinFETS, both types are sensitive.
While all these studies initially focused on in-plane stress, the question raised about the impact of vertical stress. This was studied using a nanoindenter set-up in combination with in-situ electrical probing [7]. These experiments showed a clear impact of vertical stress in FinFETs [8], but also indicated that nanoindentation produced both in-plane and out-of-plane stress, and in these experiments FEM models were required to calibrate the stress. A nice solution to this was offered by Schlipf et al. [9,10].

Acknowledgments

All imec contributors and partners of the 3D program of imec are acknowledged. Especially all design and processing engineers providing samples, all stress-impact researchers, and the program director Eric Beyne

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In-situ nano-XCT study of the local energy release rate for crack propagation in advanced ICs

Kristina Kutukova[1]*, Jürgen Gluch[2], Matthias Kraatz[2], André Clausner[2], Ehrenfried Zschech[1]

[1]deepXscan GmbH, Zeppelinstr., 01324 Dresden, Germany
[2]Fraunhofer Institute for Ceramic Technologies and Systems IKTS, Maria-Reiche-Str. 2, 01109 Dresden, Germany

**kristina.kutukova@deepxscan.com*

Recent developments in transmission X-ray microscopy (TXM) and high-resolution X-ray computer tomography (nano-XCT) make in-situ studies of microcrack evolution in 3D nanopatterned systems, e,g, in fully integrated backend-of-line (BEoL) interconnect stacks of ICs, possible [1]. Merging high-resolution nondestructive 3D imaging and a miniaturized micromechanical test allow to study the fracture behavior of Cu/low-k stacks and to determine local mechanical properties of materials at the micro- and nanoscale.

In this study, two miniaturized piezo-driven double cantilever beam (micro-DCB) test set-ups were applied in a laboratory TXM (photon energy 8 keV) to study in-situ microcrack opening and propagation in the Cu/low-k BEoL stack of a microchip manufactured in 14 nm CMOS technology node [2]. For both micromechanical testers, image analysis procedures were developed and applied, and the local energy release rate G at the crack tip was determined for sub-100nm regions, by extending the classical fracture mechanics to small dimensions.

During the micro-DCB test at the miniaturized sandwich-like sample, the geometry of the microcrack was imaged with about 100 nm resolution at several loading steps. The subsequent data analysis - applying linear elastic fracture mechanics and the Euler-Bernoulli beam model - allowed to determine the critical energy release rate G_c for crack propagation in sub-100 nm regions of a BEoL stack quantitatively. Particularly, G_c was experimentally determined at the crack tip for different regions of the wafer: in the scribe line (SR), near the metallic guard ring (GR) structure and in the patterned Cu/low-k interconnect stack. It was shown that the GR structures significantly increase the critical energy release rate G_c for crack propagation compared to the values in patterned surrounding regions, and it is about one order of magnitude higher than the G_c values measured for the respective unpatterned dielectric thin films.

The determination of local mechanical properties of materials as described in this study allows to evaluate process-induced materials changes and it provides a pathway to study the scaling of mechanical properties of interconnect stack materials of advanced ICs. The experimental results gathered at realistic interconnect structures provide valuable information to control the fracture path in the BEoL stacks and for the design of guard ring structures to ensure the requested mechanical robustness of advanced ICs.

Acknowledgments

The authors thank Han Li, Intel Inc, Hillsboro/OR, USA, for valuable discussions. Financial support from SRC under Member-Specific Research Contract P30697 is greatly appreciated.

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T5

Indentation-induced delamination and adhesion work evaluation at elevated temperature in industrial semiconductors

Pal-Jen Wei[1]*

[1]*Bruker, 3F-3, No. 6, Taiyuan 1st street, Zhubei City, Hsinchu 30288 Taiwan*

**Pal-Jen.Wei@bruker.com*

Film adhesion is critical to the performance of semiconductor devices, with interfacial delamination and fracture nearly always leading to device failure. Here, indentation tests were applied to thin film devices in order to induce stresses to cause delamination. A discontinuity in the load-displacement behavior "pop-in" indicates a critical stress to cause interfacial delamination. The loads at these pop-in events are found to have a proportional relationship with the critical load results of the more common scratch test, providing a basis for converting critical forces from the two methods. Nanoindentation, combined with a variable temperature stage that provides a stable and uniform micro-environmental chamber, allows for the probing of critical forces throughout the temperature range of expected device operation.

The delaminated region that occurs after the unloading of the indentation results in a region that bulges from the original surface, as the film is suspended over the substrate. This region can be measured using SPM or optical imaging of the region, and a radius of delamination, r, and the contact radius, a, can be obtained. This information, combined with the film hardness, H, and modulus, E, determined from standard nanoindentation tests at forces lower than result in delamination, allow the calculation of the strain energy release rate, G, through the following equation.

[1].

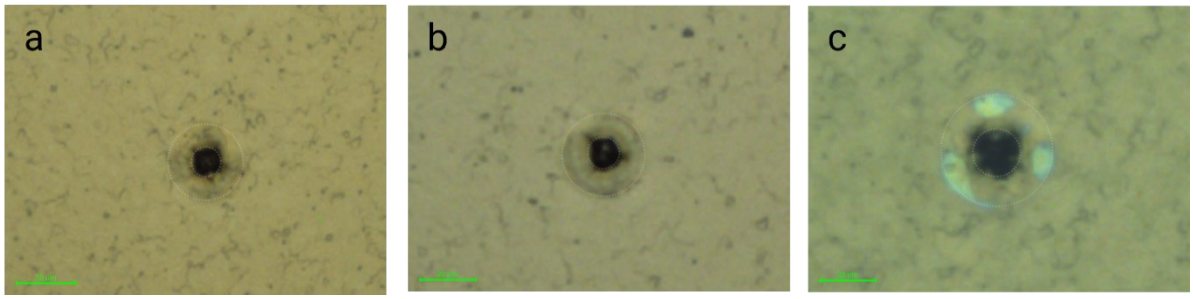

Figure 1. Optical images of indentation-induced delamination of polyimide/copper interface for determination of contact radius and delaminated radius at (a) 35ºC; (b) 150ºC; (c) 215ºC.

References

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Piezoresistive Characteristics of MOSFET Channels Determined with Indentation Stress-induced Ring Oscillator Parameter Shifts

André Clausner[1]*, Simon Schlipf[2], Jens Paul[2], Simone Capecchi[2], Christoph Sander[1], and Ehrenfried Zschech[3]

[1] *Fraunhofer IKTS, Maria-Reiche-Str. 2, 01109 Dresden, Germany*
[2] *GLOBALFOUNDRIES Dresden, Germany*
[3] *deepXscan Dresden, Germany*

**andre.clausner@ikts.fraunhofer.de*

The mechanical stress/strain-related changes in the characteristics of transistors manufactured in the 22 nm node of the fully depleted silicon on insulator (FDSOI) CMOS technology is studied with advanced experimental indentation designs. Precisely, NAND and NOR ring oscillator circuits are used to monitor the strain-caused charged carriers mobility changes in the silicon transistor channels. Piezoresistive coefficients for strained silicon are then calculated from the experimental indentation data using spherical [1] and cylindrical [2] tip geometries as well as for comparison four-point bend (4PB) experiments [3]. In contrast to spherical tips, cylindrical indentation tips as well as 4PB experiments enable to induce the mechanical stresses and strains more selectively into a specific spatial direction. To set up the experimental details appropriately, numerical Finite Element Method (FEM) simulations of the experimental designs have been used. Additionally, FEM studies are conducted to compute the quantitative stress and strain values in the silicon transistor channels as a function of contact load as well as chip and tip geometries, see Fig. 1. Using the signal deviations of the RO circuits subjected to these quantitative strain and stress data from spherical and cylindrical indentation (derived by FEM), a set of equations using the linearized piezoresistive model are created to determine the directional piezoresistive coefficients [4].

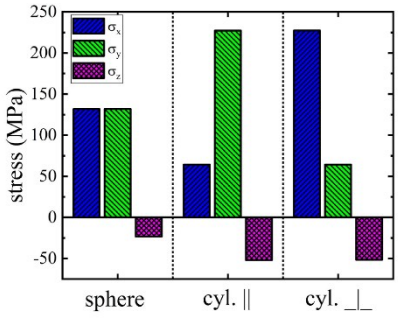

Figure 1. FEM computed normal stress tensor components in the ring oscillator structures for spherical and cylindrical indentation experiments.

Acknowledgments

The presented work has been created within the IPCEI projects RingO and RingO2 conducted in close collaboration with GLOABALFOUNDRIES Dresden and the excellent PhD work of Simon Schlipf.

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Hybrid Dielectric Films for Device Technologies: Understanding Relationships between Molecular Structure, Processing and Function

Reinhold H. Dauskardt*, Karsu I. Kilic

[1] *Department of Materials Science and Engineering Stanford University, Stanford, CA 94305*

**dauskardt@stanford.edu*

Emerging interconnect technologies with increased performance of microchips necessitate the reliable integration of ultra-low-k dielectric materials such as hybrid organosilicate glasses (OSG) as insulating units to prevent crosstalk. However, the process of obtaining nanoscale trench patterns densely filled with low-k dielectrics between conducting units has been challenging as the feature sizes become smaller. One of the main challenges is the undesired formation of low density regions in the low-k dielectric material filled inside the gap which complicates the proper scalability of low-k dielectric materials, as well as leading to poor device reliability.

Using molecular dynamics simulations, we work to develop computational modeling strategies where we explore the way different hybrid OSG precursors pack under nanoscale confinement and interact with the trench material to understand the role of precursor structure and OSG-trench interaction on the formation of low density. This will ultimately guide experimental efforts in terms of precursor selection to achieve controlled density to enhance mechanical reliability. Our simulation results show that *hyperconnected* and *cyclic* 1,3,5-benzene precursor molecules pack more homogeneously under nanoscale confinement compared to precursors such as conventionally connected Et-OCS (ethylene bridged) molecules (**Fig. 1**). We demonstrate that the more homogenous distribution and better crosslinking abilities of hyperconnected 1,3,5-benzene precursors under confinement together lead to the formation of more uniform filling and better connectivity of the hybrid material formed inside the feature; thereby yielding improved elastic and fracture properties compared to the hybrid OSG derived from precursors such as the Et-OCS molecule.

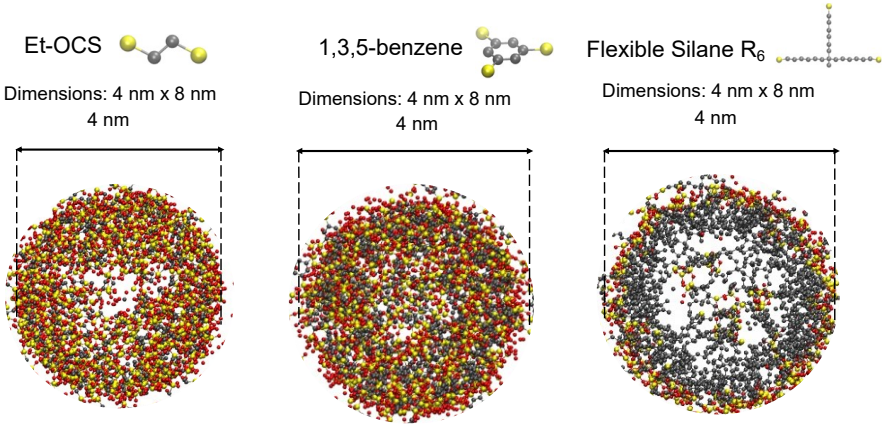

Fig. 1: Molecular morphology of low-k dielectric organosilicate fillings derived from Tt-OCS, 1,3,5-benzene and flexible silane precursors. The gap aspect ratio was 1:2 and the gap depth 4 nm. 1,3,5-benzene molecules result in more uniform density compared to Et-OCS and flexible silane molecules.

Acknowledgments

The work was supported in part by the Semiconductor Research Corporation (SRC).

T9

Solid-phase bonding process using nanostructured surface for power devices in automotive

Hiroshi Nishikawa[1]*

[1]*Joining and Welding Research Institute, Osaka University, 11-1 Mihogaoka, Ibaraki, 567-0047 Osaka, Japan*

**nisikawa@jwri.osaka-u.ac.jp*

Wide bandgap (WBG) semiconductors, such as SiC and GaN, are being developed as promising replacements for Si-based semiconductors because they have high power density, operation frequency, and break down voltage. These WBG semiconductors can operate efficiently at temperatures above 300 °C. Compared with the conventional silicon (Si) device, the SiC device can operate with significant lower power loss and higher operating temperature, which contributes to miniaturization and higher performance of power modules. To assemble these devices, the high-temperature bonding process as a die bonding process is one of the key technologies. Then, the EU RoHS directive currently exempts the use of high-lead-containing solders such as Pb-5Sn and Pb-10Sn solders in electronic packaging. However, there is no guarantee that the exemption will last. A strong drive thus exists to find lead-free alternatives for the SiC power devices. Recently, sintering metallic nanoparticles such as Ag and Cu have been explored by virtue of their high melting temperatures and superior electrical and thermal conductivities [1, 2]. However, the nanoparticle paste contains various organic substances. During the bonding process, residual organic materials can induce the formation of unexpectedly large voids or gaps in the joint layer. The nanoparticle paste has some problems for practical use. To avoid the problems, we have proposed a solid-state bonding process without solvents using a metal sheet with nanostructured surface [3]. In this talk, I will introduce new approach on die bonding materials and processes using the metal sheet with nanostructured surface. I will introduce a manufacturing process of nanoporous sheets in dealloying [4] and a pressure-assisted nanoporous bonding (NPB) for die bonding process. Basic experimental test results such as joint strength and interfacial behavior with a substrate will be also explained. For example, nanoporous Cu (NPC) sheets were fabricated from Mn–Cu precursor sheets with thicknesses of 110–120 μm. The NPC sheet was prepared using the dealloying method, which involved the selective dissolution of Mn into 4 % hydrochloric acid from the Mn–Cu precursor. XRD patterns of the precursor sheet and the as-dealloyed NPC sheet are shown in Fig. 1(a). Furthermore, the surface morphology of the NPC sheet (ligament size = 132 nm) fabricated by dealloying a precursor sheet is illustrated in Fig. 1(b).

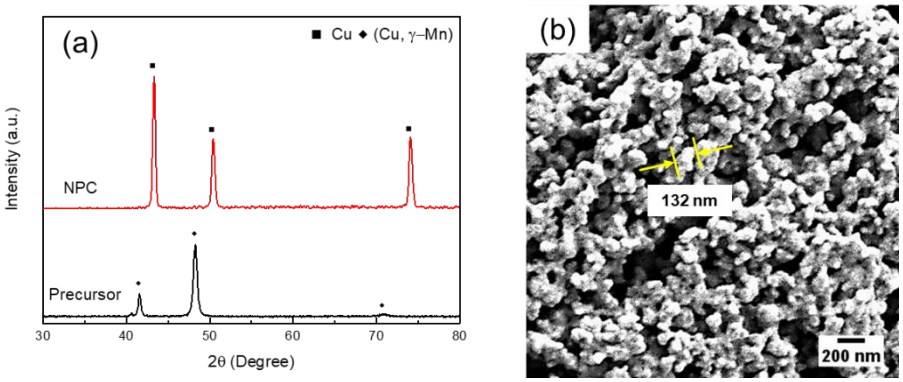

Figure 1. (a) XRD patterns of the precursor sheet and as-dealloyed NPC sheet. (b) SEM images of the structure of the as-dealloyed NPC sheet.

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Hybrid bond and nanowired bump technologies for high density interconnect formation on wafer level

Iuliana Panchenko[1,2,*], Laura Wenzel[1,2], Steffen Bickel[1,2], Adil Shehzad[1], Maik Mueller[2], Catharina Rudolph[1], Sebastian Quednau[3], Olav Birlem[3], Andreas Graff[4], Frank Altmann[4], Manuela Junghähnel[1]

[1] Fraunhofer IZM ASSID, Ringstr. 14, Moritzburg, [2]Institute of Electronic Packaging Technology, TU Dresden, Helmholtzstr. 10, Dresden, [3] NanoWired GmbH, Emanuel-Merck-Str. 99, Gernsheim, [4] Fraunhofer IMWS, Walter-Hülse-Str. 1, Halle

**iuliana.panchenko@assid.izm.fraunhofer.de*

This study starts with an overview of different fine-pitch interconnect technologies, which are based on solder (Cu pillar with solder cap, solid-liquid interdiffusion bonding) and pure Cu metal (Cu/Cu thermo-compression and ultrasonic bonding, Cu/SiO_2 hybrid bonding, nanowired bump). Those technologies are required for the packages with high I/O number and especial for heterogeneous 2.5D or 3D chiplet integration. The application fields are consumer electronics, high-performance computing, artificial intelligence, etc. The advantages and disadvantages of these interconnect technologies as well as process flows will be addressed. The recent demand in chiplet integration is a combination of at least two different interconnect technologies for the bonding on one interposer, which requires changes in a current process flow.
The result chapter of this study is an overview of two Cu interconnect technologies for wafer level based on hybrid bond pads and nanowired bumps. Both are excellent candidates for small interconnect diameters between 3 µm and 25 µm. Nanowires used for the bumping process were 100 nm and 200 nm in diameter. Hybrid bond processing requires a demanding chemical-mechanical planarization, particle-free dicing technology (in case of die-to-wafer bonding) and surface activation. We report on bonding results both for wafer-to-wafer and die-to-wafer, as well as detailed microstructure (grain orientation analysis by Electron-Backscatter-Diffraction, EBSD) characterization of the bonded interconnects (Fig. 1a) [1]. The nanowired bump processing has several simplifications against the hybrid bond pad preparation, however it needs an alternative process for the removal of the Cu seed layer. We report on the proposed process flow and die-to-die bonding results [2], as well as microstructure of the nanowired bumps (Fig. 1b). We also address the high-resolution TEM results of the Cu nanowired interconnects.

a) Hybrid bond interconnect (ø4µm top pad) – EBSD map

b) Nanowired Interconnect (ø25µm top bump) – SEM image

Fig. 1 Exemplary images of the microstructure of the hybrid bond interconnect (a) and nanowired interconnect (b)

Acknowledgments

This study is an overview of two comprehensive wafer level interconnect technologies at fine scale, therefore we acknowledge the whole staff of Fraunhofer IZM ASSID involved in the wafer processing. Financial support for this study was provided over following projects: “Functional Integration for Micro-/Nano-Electronics” under Grant 100245395 and Grant 100249378 and “Transfer center: Functional Integration for the Micro-/Nano-Electronics” under Grant 100368159 and Grant 100368161, “Wafer Metrology Center” EU project 16ME0057, “NanoInt” Fraunhofer SME internal project.

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Phase change materials for embedded memories: *in situ* investigation of crystallization behavior using synchrotron radiation

Olivier Thomas[1]*, Philipp Hans[1], Cristian Mocuta[2], Christophe Guichet[1], Y. Le-Friec[3], P. Boivin[4], R. Simola[4], P. Noé[5], S. Jeannot[3]

[1] *Aix Marseille Univ, Univ Toulon, CNRS, IM2NP UMR 7334, Marseille, France*
[2] *Synchrotron SOLEIL, L'Orme des Merisiers, Saint-Aubin - BP 48, 91192 Gif-sur-Yvette Cedex, France*
[3] *STMicroelectronics, 850 rue Jean Monnet, 38920 Crolles, France*
[4] *STMicroelectronics, 190 Ave Coq, 13106 Rousset, France*
[5] *Université Grenoble Alpes, CEA-LETI, MINATEC, 17 rue des Martyrs, 38054 Grenoble, France*

**olivier.thomas@univ-amu.fr*

Phase Change Memory is a very promising non-volatile memory that is being considered by several companies for a wide range of applications (storage-class memory, in-memory computing, neuromorphic computing, eNVM for microcontrollers …). Among Phase Change Materials (PCMs) the ternary Ge-Sb-Te phase diagram offers a rich variety of interesting phases including the much-studied compounds $Ge_2Sb_2Te_5$ and GeTe. At STMicroelectronics a new Ge-rich Ge-Sb-Te alloy (GGST) has been developed with a crystallization temperature above 350°C [1] for addressing the specific needs of the automotive market where high operating temperatures are required.

During the last years we have investigated the crystallization and mechanical behavior of these PCMs using X-ray diffraction as a function of temperature during annealing. Capped thin films are heated *in situ* under nitrogen atmosphere [2,3,5] on the DiffAbs beamline of SOLEIL synchrotron facility. The incident beam is monochromatic (18 keV) and the incidence is fixed. A bidimensional detector collects the diffraction pattern and is corrected and integrated [4] to yield a 1D diffraction pattern. The diffraction peaks are then fitted with an analytical function that allows extracting the integrated intensity, integral breadth and position of the Bragg peaks. These parameters allow following the crystallization kinetics and the thermomechanical behavior [2,3] of thin films as a function of various parameters: doping, film thickness (5 nm – 50 nm), nature of surrounding layers … In addition, we will show that, thanks to the high flux and penetrating power of synchrotron X-rays, patterned and metallized structures close to real products can be investigated. The results obtained from such *in situ* investigations bear important consequences for the understanding of the crystallization process in memory cells.

Acknowledgments

The authors gratefully acknowledge the SOLEIL Synchrotron for allocating beam time. P. Joly, is acknowledged for excellent technical support during the experimental campaigns at SOLEIL Synchrotron on DiffAbs beamline. This research was supported partly by IPCEI/Nano 2022 program and by ANR under contract SESAME ANR-15-CE24-0021.

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Controlled microcrack steering into toughened regions – What microelectronics can learn from nature?

Ehrenfried Zschech[1]*, Martyna Strag[2], Kristina Kutukova[1]

[1]*deepXscan GmbH, Zeppelinstr. 1, 01324 Dresden, Germany*
[2]*Military Institute of Armament Technology, Prymasa Stefana Wyszyńskiego 7, 05-220 Zielonka, Poland*

**ehrenfried.zschech@deepxscan.com*

The advent of evolutionary developmental biology in the final decades of the 20th century was based on the fact that biologists – together with architects and engineers – established a theoretical basis for the science of form. Modern morphological research (see e.g. [1]) has not only impact on biology but also on architecture and materials science. It provides a new interdisciplinary perspective to the design of materials. The transfer of biological principles into architecture and material design has a huge potential in solving technical problems by natural forms. In particular, the goal of biomimetics is to implement a biologically informed material system that relies equally on construction principles in nature and those in fabrication [2].

A proven "damage-tolerant design" of nature are biocomposites that contain components with high fracture toughness. As an example, high-resolution X-ray imaging of the outermost layer of a mollusk shell shows that the propagation of microcracks that have been initiated by an indent are steered into and finally trapped in an amorphous organic phase with high fracture toughness, located between calcite building blocks [3]. Studies at biological objects, combining experimental data and modeling, can help to develop fracture mechanics at small scales and to understand microcrack propagation in hierarchically structured material systems.

Learning from nature, an approach for avoiding mechanical damage of microchips manufactured in leading-edge CMOS technology nodes is a controlled steering of microcracks, e.g. generated during the wafer dicing process, into regions with relatively high fracture toughness [4]. One option to prevent material cracking and interface delamination in BEoL stacks is the integration of metallic guard ring (GR) structures at the rim of the microchip. These specially designed metal structures are integrated into BEoL stacks to dissipate energy in such a way that crack propagation is efficiently slowed down and eventually stopped. Experimentally, a displacement-controlled crack propagation through the Cu/low-k stack and a controlled crack steering were realized in a miniaturized piezo-driven double-cantilever beam (DCB) test, by a combination of loading modes, i.e. a tuned fracture mode mixity locally at the crack tip. This mechanical test set-up was positioned in the beam path of a laboratory transmission X-ray microscope (TXM) for imaging the pathways of microcracks with sub-100nm resolution in the region of interest (ROI) that includes the BEoL and particularly the GR structures [5]. With the methodology described, i.e. the controlled steering of microcracks into regions with high fracture toughness while considering nanoscale mechanical properties of fully integrated 3D interconnect stacks (particularly the local critical energy release rate G_c), conclusions for the robustness of BEoL stacks can be drawn and input for the design of GR structures can be provided [6].

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Degradation mechanisms of 10kV-reinforced isolated gate drivers at high switching frequencies greater than 30kHz

Matthias Stecher[1)*], Leonard A. Dissado[2)]

[1)]*Infineon Technologies, 85579 Neubiberg, Germany*
[2)] *Prof. Emeritus, Dep. of Eng., Uni. of Leicester, Uni. Road, Leicester, LE1 7RH, U.K*

**Matthias.Stecher@infineon.com*

Galvanic isolated couplers are commonly used in industrial, telecom and automotive systems to counteract ground potential differences and to protect the user against high voltage shock. Hence, the robustness of the galvanic insulation of couplers has to be guaranteed over the operating life of the equipment. The design of such equipment is a challenging task because, for example, even an AC/DC power converter for a home appliance (e.g. a laptop computer) has to withstand not only the 220V system voltage, but also the PWM (pulse width modulation) recurring peak voltages reaching several hundred volts, overvoltage occurrences due to power grid instability and surge pulses (1.2µs rise-time and 50µs fall-time) generated due to lightning outside the home. These power grid disturbances can reach several thousand volts at the 220V-AC side of the power converter. To guarantee the robustness of such appliances they must be certified by independent test houses such as the VDE, TUEV or UL. The certification is performed on the basis of several standards, such as the IEC 60664 (Insulation coordination for equipment within low-voltage systems), IEC 62368 (Safety requirements for audio/video, information and communication technology equipment) and IEC 60747-17 (safety requirements for magnetic/capacitance couplers). According to these standards, all PWM applications running below 30kHz can be certified via voltage tests at 50Hz. Above 30kHz the dielectric insulation thickness has to be increased by a factor of two at minimum.
The typical IC coupler design solution consists of two chips, one for the primary and the other one for the secondary side [1]. Each chip is placed on its own lead-frame paddle within a molded IC package. A high-voltage capable transformer or capacitance is placed on one or both of these two chips to provide a signal path between the primary and secondary sides. The connection between the chips is done by bond-wires via the top winding/electrode of the transformer/capacitance. The dielectric material and the thickness between the paddles and within the transformer/capacitance must be chosen to withstand several thousand volts. The typical SiO2 isolation thickness in the transformer/capacitance is between 10 and 30µm for PWM applications running below 30kHz. There is also a parasitic E-field above the transformer/capacitance which stresses the mold compound above the chip passivation. This can reach several 100V/µm.
To increase the power efficiency, the PWM switching frequency has been increased from 30kHz up to several hundred kHz in recent years, thanks to the introduction of GaN and SiC power transistors. The above-mentioned standards already require for a 100kHz PWM application a 2-4 times thicker isolation than that for an 30kHz application. Whether this required thickness increase is justifiable has been analyzed based on material test structures stressed using high voltages (3-10kV) and high frequency (30, 150, 450, 800kHz) for very long periods of time. The results indicate that the life-time of the coupler at high voltages is determined by the SiO2 within the transformer/capacitance while at medium voltages the determining factor is the mold-compound on top of the chip. The experiments furthermore show that the life-time actually increases with increasing frequency, suggesting therefore that a thicker isolation than the one used for a 30kHz application is not needed. For both the SiO2 and the mold compound a threshold E-field can be determined, below which the main degradation mechanism is not even visible. This presentation will provide details of the experiments, results and possible degradation models.

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Contrasting Stress Evolution During Lithiation and Delithiation of Different Electrode Materials for Thin Film Batteries

Carl V. Thompson[1]*, Lin Xu[1], Michael J. Chon[1]

[1]*Department of Materials Science and Engineering, Massachusetts Institute of Technology, Cambridge, MA 02139, USA*

**cthomp@mit.edu*

Thin film Li-ion batteries with high energy capacity and cyclability are needed for autonomous microsystems such as sensors used for a wide range of applications in the Internet of Things. Silicon and germanium can serve as high capacity anodes, and for applications in microsystems, RuO_2 can serve as a high capacity cathode. The high Li capacity of these materials causes volume expansions of 250-300% that can lead to mechanical failure and poor cyclability. In-situ measurements show that compressive and tensile stresses of order 1 GPa develop in Si and Ge (Fig. 1(a), [1]). However, the behavior of RuO_2 is fundamentally different, with low tensile stresses during the 2nd and subsequent delithiation cycles and a more gradual increase in the compressive stress during lithiation (Fig. 1(b), [2]). Using lithographically patterned arrays of notched holes in RuO_2 films, this behavior was shown to be associated with reversible sliding at the interface between RuO_2 and the underlying current collector (Fig. 3(c), [3]). Regular arrays of channel cracks formed at locations controlled by the notched holes, leading to formation of square islands of RuO_2 film. In subsequent cycling, these wide channel cracks reversibly closed and opened during lithiation and delithiation.

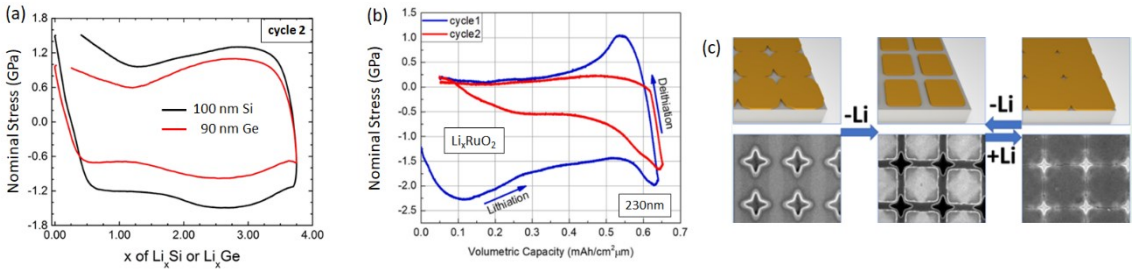

Figure 1: a) Nominal stress measured in situ during lithiation/delithiation cycles of (a) Si and Ge films and (b) a RuO_2 film. (c) RuO_2 films patterned with an array of notched holes. Channel cracks form to create square islands of RuO_2. Subsequent cycling causes the channel cracks to reversibly close and open.

Acknowledgments

This research was supported by the National Research Foundation, through the Singapore-MIT Alliance for Research and Technology (SMART).

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Tortuosity and Porosity in Electrochemical Systems - Computed Tomography Based 3D Transport Modelling

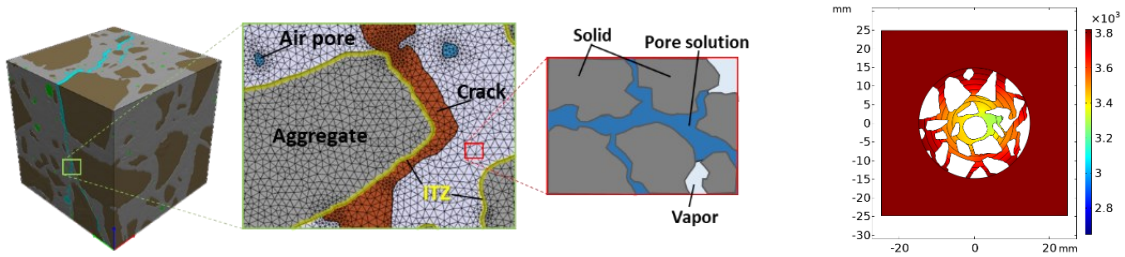
Robert Filipek[1]*, Ehrenfried Zschech[2]

[1]*AGH University of Science and Technology, Faculty of Materials Science and Ceramics, al. Mickiewicza 30, 30-059 Kraków, Poland.*
[2]*deepXscan GmbH, Zeppelinstr. 1, 01324 Dresden, Germany.*

**rof@agh.edu.pl*

Even up-to-date advanced studies of the transport and reactions in electrochemistry are characterized either by essentially homogeneous treatment of the system (with possible including several species, ions and neutral molecules) with non-linear electrode kinetics (Butler-Volmer or Tafel equations) or by a more sophisticated treatment of the system (including its real micro-structures), but with a simple transport model (one species only and simple Fickian diffusion).

Two examples will illustrate a new more general attempt for the description of transport and reactions in electrochemical systems. The first example concerns the influence of ions activities and materials structure on ions transport, a problem of a fundamental importance for safety of reinforced concrete structures, in particular for understanding and minimizing corrosion of rebars in concrete. The second example demonstrates the influence of the material's porosity and its 3D microstructure on the infiltration of the material. The Navier–Stokes and mass balance equations are solved in the continuous porous structure and the results are compared with simplified simulations which assume a homogeneous material and with average properties (porosity, tortuosity and constrictivity) accounting for its complex morphology.



(a) (b)

Figure 1. (a) 3D hierarchical concrete structure; (b) Chloride ion concentration in concrete sample (2D cross-section).

Concluding, the influence of material's nano-/micro-structure on transport in real 3D electrochemical systems and processes is presented. The geometry for the transport is taken from X-ray computed tomography (XCT) measurements. The XCT results are analysed and using specialized algorithms a segmentation of 3D structure is performed which is used for 3D mesh generation. The mesh prepared in this way is then utilised in finite element method simulations using COMSOL Multiphysics software and user defined governing equations.

Acknowledgments

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Reliability and Recycling of Battery Materials

Jörg Acker*, Thomas Langner, Tim Sieber and Anja Rietig

Brandenburg University of Technology Cottbus-Senftenberg, Department of Physical Chemistry, 01968 Senftenberg, Germany

**joerg.acker@b-tu.de*

Spent lithium-ion batteries (LIB's) are not only a waste object that requires proper disposal due to the hazards emanating from them, but also serve as a source of raw materials with an enormously important economic value for the future of electromobility and energy storage technology.

Today, the vast majority of end-of-life LIBs are still recycled using the pyrometallurgical process, in which complete LIBs are melted in a smelting furnace and the most valuable components, cobalt and nickel, as well as copper (from the substrate foils of the anodes), are recovered as a metallic melt. To recover lithium from slag, on the other hand, requires the effort of "slag design" to convert the lithium into a stable compound that can be easily separated from the rest of the slag.

The second important recycling route is hydrometallurgical processes. The starting point for this is the so-called black mass, which consists of cathode material, anode graphite, conductive carbon black and binder. To recover the black mass, batteries are disassembled to the level of cell stacks or individual cells, and then mechanically crushed. Multi-stage separation processes yield the black mass, which, depending on the process, contains impurities of aluminum, copper and plastic residues. The black mass is dissolved in acidic reagents and, after complex precipitation and extraction processes, nickel, cobalt and nickel are recovered in the form of pure salts, typically as carbonates.

A new, alternative approach is functional recycling, in which the cathode material is recovered from end-of-life LIB's in such a way that its chemical and physical functionality is preserved. This means designing the process so that the particle shape is maintained, the material is not dissolved, the high oxidation states (+4) are preserved, and side reactions that attack the material or cause changes to the particle surface are suppressed. The goal is to recover the material at such a high quality that it can be used as an admixture to virgin material in the production of new batteries.

However, functional recycling introduces a variety of challenges that begin with the first step of recycling, the deep discharge of the batteries. Deep discharge means the almost complete transfer of lithium ions from the graphite anode, since lithiated graphite has a similar high chemical reactivity as elemental lithium. The second challenge is the contact of the opened batteries with the ambient air. Here, the volatile components of the electrolyte evaporate, while the low-volatile components and the conducting salt, typically $LiPF_6$ but also other compounds, remain on the cathode surface. The latter decompose in the presence of atmospheric moisture and initiate a variety of degradation processes on the material.

In the talk, some of the most important aspects and results of functional recycling will be presented, as well as the first industrial process based on this principle. Finally, a brief outlook on the future challenges raised by very nickel-rich cathode materials will be given.

Strains and stresses control in microelectronic devices: how to optimize the steps from design to manufacturing ?

Lionel Vignoud*
Univ. Grenoble Alpes, CEA Leti, Grenoble, France
**lionel.vignoud@gmail.com*

Introduction: the control of strains and stresses in the design and manufacture of microelectronic devices is crucial to guarantee performance and reliability. To obtain a functional device, it is therefore necessary to control these parameters during each of the manufacturing steps. At CEA-DRT (Leti) we are currently developing a broad expertise on this topic based on experimental works coupled with simulation and theoretical approaches. By determining the thermomechanical properties of materials and integrating these properties into an analytical model developed at CEA-DRT (Sigmapεps), we are able to predict the effect of whole thermal history of the multilayer system as well as processing conditions which are taken into account for each layer. For the processing of a functional device, stresses and strains are therefore optimized during all technological steps.

Characterization: at room temperature, a dual confocal chromatic sensor allows to measure films thicknesses and the reference bow of wafers. Stress determination at high temperature is performed with a multi-beam optical sensor coupled with a rapid thermal anneal (RTA). Then, thermomechanical properties are obtained by comparing several methods: thermally induced stress, dynamic mechanical analysis (DMA) or nanoindentation technics. Metals, oxides and polymers thin layers mechanical properties are predicted with these approaches.

Analytic simulation (Sigmapεps): the developed model is based on the theory of elasticity and was originally presented by Hutchinson [1] then Isselé. To simulate these processes step, we consider three strain contributions in the material: the intrinsic strain related to the deposition, the thermal strain due to the thermal budget undergone by the material, and the elastic strain generated by the material to accommodate these inelastic deformations and reach a state of mechanical equilibrium. Working on this model and equations allows to obtain the equation of the stress within each layer (substrate or film) [2].

Application for an interposer device: we worked with this model for optimizing the conception and the manufacturing of interposers (Figure 1). Chips transferred on the front side are connected at 260°C, thanks to metal interconnection pads (micro-bumps).

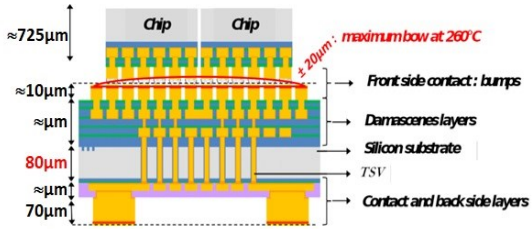

Figure 1. Sectional view of an interposer

The interconnection network consists of several films and a passive layer to protect the lower layers. Our simulation allows to estimate the variation for each process step and determine the final bow at 260°C.

The experimental measurements confirm the simulation (Figure 2). Therefore, every manufacturing step is then optimized.

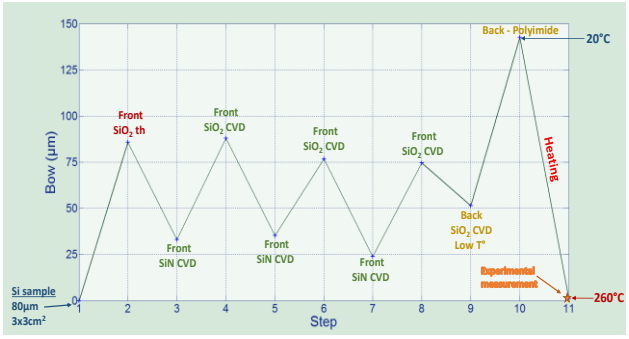

Figure 2. Simulated bow for an interposer at each process steps.

Acknowledgments
Part of this work, carried out on the Platform for Nanocharacterisation (PFNC), was supported by the "Recherche Technologique de Base" program of the French National Research Agency (ANR).

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Advancing nanoscale characterization of semiconductor devices by effort-less 4D-STEM workflows

Daniel Němeček[1]*, Robert Hooley[1], Tomáš Morávek[1], Narendraraj Chandran[1]

[1]*TESCAN ORSAY HOLDING, Libušina třída 21, Brno, Czech Republic*

**daniel.nemecek@tescan.com*

Continuous development of new semiconductor devices is driven by the demand for faster data processing, faster signal transmission, greater storage capacity, and continuously decreasing power consumption. Achieving such performance improvements is dependent on increasing the density of the active elements and cutting the signal path in semiconductor devices. Consequently, semiconductor manufacturers are challenged when characterizing chemistry and morphology at specific sites on ever smaller devices. It is beneficial to employ comprehensive and complementary analytical methods, measuring chemical and structural properties as well as specimen morphology, down to the sub-nanometer scale.

4D-STEM is a powerful analytical method based on nanobeam diffraction that can resolve and characterize distribution of crystalline phases and orientations of individual grains in different layers of semiconductor devices at the nanoscale level. These analyses are critical because the electrical performance of devices depends strongly on the type and distribution of crystalline phases in the device layers. However, broader adoption of 4D-STEM techniques has been limited by complexity of experimental setups and challenges with synchronization of sample scanning by an electron beam with beam blanking, beam precession and readout of a pixelated detector. In this presentation, we will show a new approach to acquisition and processing of 4D-STEM datasets quickly and with minimal user input due to full integration of all needed hardware components with high levels of system automation and optimization algorithms for on-the-fly data processing and visualization of results.

The power of 4D-STEM characterization will be demonstrated on identification of phases in a device that contained anomalies in the GST layer that could not have been revealed by using the standardly used analytical methods such as EDX elemental mapping. Additionally, application of 4D-STEM techniques to visualize and quantify Lagrange strain in user defined tensile directions, shear and pattern rotation at the interface between different device layers will be shown. A 4D-STEM strain map taken from a $Si_{0.8}Ge_{0.2}$ epitaxial film on a silicon substrate displayed a tensile strain within the gradient at the interface between the silicon and $Si_{0.8}Ge_{0.2}$ layer with respect to the silicon substrate. The strain values were calculated based on a user defined reference pattern from an unstrained region using a fully automated procedure with on-the-fly data processing, which is accessible to all operators of analytical instruments. These kinds of analyses and measurements are useful for the quantification and observation of desired strains for strain engineering as well as for failure analysis where undesirable strain is present.

Acknowledgments

We are grateful to STMicroelectronics (Grenoble, France) for providing a semiconductor device for the multimodal phase and orientation analysis used in this study.

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Recent advances in nanoscale strain mapping using 4D STEM

Christoph Gammer[1]*, Lukas Schretter[1], Simon Fellner[1], Alice Lassnig[1], Jürgen Eckert[1,2]

[1]*Erich Schmid Institute of Materials Science, Austrian Academy of Sciences, Jahnstraße 12, 8700 Leoben, Austria.*
[2]*Department of Materials Science, Montanuniversität Leoben, Jahnstraße 12, 8700 Leoben, Austria.*

**christoph.gammer@oeaw.ac.at*

Transmission electron microscopy (TEM) has provided great insight into structural properties of materials. Of fundamental importance is the local stress, that controls functional properties of modern devices and fundamentally defines deformation in materials. Stress fields can show a heterogeneous distribution at the nanoscale, requiring measurement techniques that offer both, high spatial resolution and high precision [1]. For very thin samples, that can be oriented in a zone axis, atomic resolution high-angle annular dark-field (HAADF) scanning TEM (STEM) can be used to directly image the atomic lattice. As an alternative, 4D-STEM using nanobeam electron diffraction can be used to measure the local elastic strain. Figure 1 shows the experimental setup, where a probe rasters over the sample and in addition to the HAADF-STEM image, a full diffraction pattern is recorded for every probe position. The convergence angle is chosen such that the diffracted disks are well separated. A strain map can be calculated by measuring changes in the lattice constants from the diffraction patterns. Recent advances in the speed of electron detectors and new analysis routines have enabled to map large fields of view [2]. To obtain reliable strain maps, advanced peak registration techniques need to be used, that can accurately detect the disk positions in thick specimens and that take into account the quality of each peak detection in the final strain calculation. Based on these advances, 4D-STEM strain mapping can even be performed during continuous *in situ* deformation, allowing to measure transient local strains around individual defects [3]. Finally, 4D-STEM is also applicable to amorphous materials, where strain can be determined by fitting an ellipse to the first order diffraction ring [4]. We will discuss future efforts for making 4D-STEM mapping a more universal and reliable technique for strain-mapping in complex materials. This includes improved experimental techniques and new analysis routines.

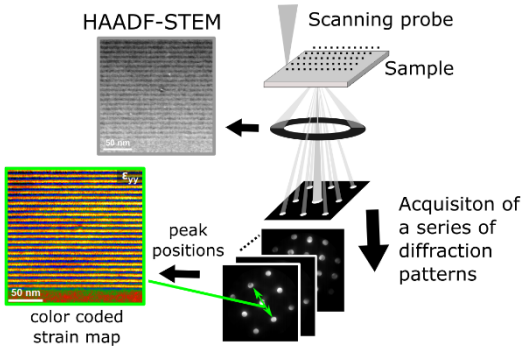

Figure 1. During acquisition of a HAADF STEM image, a diffraction pattern is acquired for every probe position. A strain map is obtained by measuring changes in the lattice constants.

Acknowledgments

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Eco-Strategies for Next Generation Electronics

Rodrigo Martins*, Guilherme Ferreira, Elvira Fortunato, Suman Nandy

CENIMAT/i3N, Department of Materials Science, NOVA School of Science and Technology, NOVA University Lisbon (FCT-NOVA) and CEMOP/UNINOVA, Campus de Caparica, 2829-516 Caparica, Portugal

**rfpm@fct.unl.pt*

In the current digital era, as the world is growing up with smart technology, on the same time our planet is drowning with huge number of unrecycled waste and environmental pollution. World is facing off the challenges against rapid climate changes and continuous ecological disturbances, caused by the revolutionary growth in socio-economic developments with fastest growing trend in smart electronics, plastic-based products and the continuous dependence on non-recyclable raw materials. On the other hand, a huge significant progress in IoT and wearable smart electronics system is demanding unremittingly portable power source. Though, there remains a lot of challenges like endless energy supply, stability, functionality and obviously biocompatibility that will promote the applications from lab scale research to industrial scale. Therefore, collectively the eco-design strategies has to ensure technological breakthroughs on multiple levels: sustainable materials design with maximum recyclable approach, low-cost-energy efficient manufacturing methods, green energy sources and integration of energy harvester into low-powered electronic platform. In that context, from decade, CENIMAT/CEMOP research center has specified their vision to build a scientific platform for future green product and make social awareness in green and sustainable technology, which could revolutionize European industry and society both with new business approach with smart sustainable lifestyle.

Figure 1. Eco-strategies for next generation materials engineering and applications

Acknowledgments

Authors acknowledge the project SYNERGY H2020-WIDESPREAD-2020-5, CSA, (proposal no. 952169) and M-ERA-NET (Project reference is M-ERA-NET3/0004/2021). This work is also partially financed by the COMPETE 2020 Programme and National Funds through FCT under the project UID/CTM/50025/2019.

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Processing flexible glass – thin film stress and its influence on glass durability

Wiebke Langgemach, Kerstin Täschner, Thomas Preußner, Morris Ott

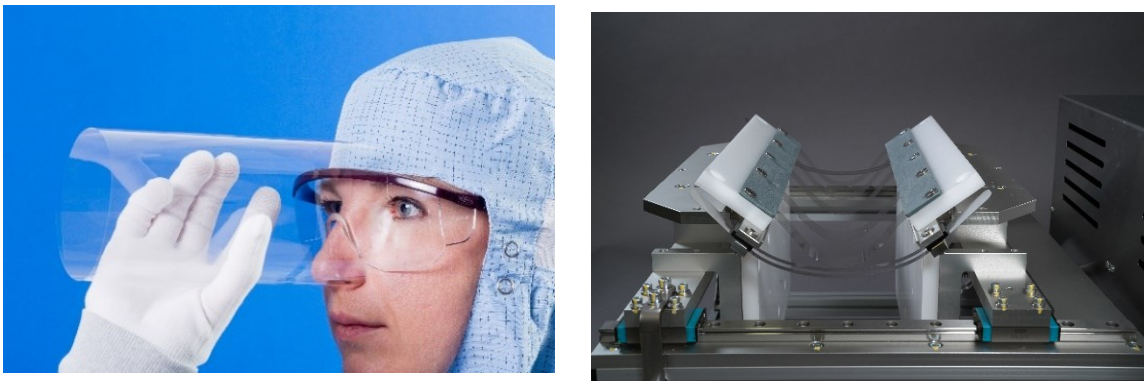
Fraunhofer Institute for Organic Electronics, Electron Beam and Plasma Technology FEP, Dresden

**wiebke.langgemach@fep.fraunhofer.de*

Ultrathin flexible glass with thicknesses of 100 µm or below is well suited for vacuum coating of thin films. It shows low surface roughness and outstanding barrier properties while being extremely bendable. The current use in foldable displays of mobile devices gives an idea of the wide range of possible applications.

However, large area coatings of flexible glass are not yet state of the art because of the higher brittleness of flexible glass compared to polymer webs. Moreover, flexible glass requires dedicated handling to mitigate potential risks during processing. Unfortunately, only little data is publicly available on the mechanical behavior of coated thin glass. Especially the influence of thin film stress on mechanical reliability has not been studied and published in detail yet. Nevertheless, experience has shown that thin film stress strongly influences the mechanical stability of the substrate glass.

In this presentation, the influence of coating parameters on the reliability of flexible glass will be discussed. Results concerning bending and early-life reliability testing will be presented and their impact upon the process chain will be discussed. These results mark the start of an extensive experimental study at Fraunhofer FEP since a detailed understanding of the mechanical reliability of the flexible glass is crucial for relevant production yields.



(a) (b)

Figure 1. (a) Glass with a thickness below 100 µm is flexible; (b) Early-life fatigue testing of flexible glass

Acknowledgments

Federal Ministry for Economic Affairs and Climate Action

Forschungsnetzwerk Mittelstand AiF EFDS

AiF – CUSTOM (Grant no. 21708 BR)

Organic semiconductors - from a lab curiosity to serious applications

Karl Leo[1]*

[1] *Technische Universität Dresden, IAPP, 01062 Dresden*

**karl.leo@tu-dresden.de*

Organic semiconductors are based on carbon compounds and allow an almost inexhaustible variety of materials. Devices based on organic semiconductors enable a variety of novel applications for flexible, lightweight, and environmentally friendly electronics. A first application success are OLED displays, which have already conquered a double-digit billion market and dominate the market in mobile phones. The doping methods developed at TU Dresden play a key role in this success.

In this talk, I introduce the material class of organic semiconductors and show with some examples from doping to organic solar cells the challenges of materials research and the implementation in products. I will discuss in some detail for the example of organic solar cells how issues like control of nanostrructures, manufacturing challenges, and lifetime issues have to be addressed. As an example for organic electronics, vertical organic transistors with greatly improved properties are discussed, including bipolar transistors which open the GHz range for organic electronics. Finally, an outlook is given for bioelectronic applications. We have recently developed devices which are used for post-surgery monitoring and will then be resorbed by the body in a controlled manner. Furthermore, I will discuss a new form of neural networks based on organic semiconductors, allowing highly efficient neuromorphic computing approaches.

Acknowledgments

I thank the many coworkers in my group and in collaborating groups for their continuous excellent collaboration and support. Furthermore, I thank SAB, DFG, BMBF, EC, and many other funding agencies for the continuous and excellent financial support.

Abstracts
-Posters-

P1

A Proactive Design Approach to Avoid Migration-Induced Failure in IC Interconnects

Susann Rothe*, Jens Lienig

Dresden University of Technology, Institute of Electromechanical and Electronic Design, 01062 Dresden, Germany, www.ifte.de

**susann.rothe@mailbox.tu-dresden.de*

Electromigration (EM) is a growing concern for IC reliability, getting more urgent with every new technology node. Due to the shrinking feature sizes, migration-robustness constraints are tightening. The well-established current-density verification in IC design is no longer sufficient to ensure migration robustness because it neglects the significant impact of interconnect geometry (e.g., length). Thus, novel stress-based models [1, 2] must be integrated in leading-edge VLSI design flows.

These models calculate the hydrostatic stress which builds up within an interconnect. They also enable us to consider other effects that gain importance for migration robustness assessment, such as thermal migration (TM) [3]. Our newly developed FEM models [4] support the simulation of the stress distribution due to EM and TM in AC interconnects.

Moreover, the rising number of nets that are at danger of migration-induced degradation leads to a tremendous amount of rework to obtain a reliable layout. To counter this alarming trend, which is getting worse with every new technology node, we propose a new, proactive design approach. It utilizes the aforementioned stress-based migration modeling and implements migration-robustness constraints already at the routing stage. Consequently, the necessary (post-layout) repair effort can be reduced drastically. Our proactive design strategy also supports full exploitation of layout-based migration countermeasures.

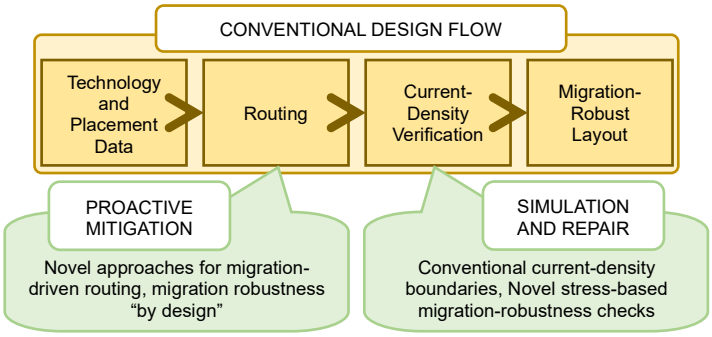


Figure 1. To address the growing challenges in migration robust VLSI layout design, novel stress-based models are applied at the verification stage. Moreover, we propose a new proactive design approach to consider migration-robustness constraints earlier – that is, in the routing step.

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P2

The Influence of the Interconnect Material on the Performance of a Highly Robust Metallization Layout

Verena Hein [1]*, apl. Prof. Dr. Kirsten Weide-Zaage[2]

[1]*X-FAB Global Services GmbH, Haarbergstr. 67 99097 Erfurt, Germany*
[2]*IMS Leipniz University Hannover, Appelstr.4 30167 Hannover, Germany*

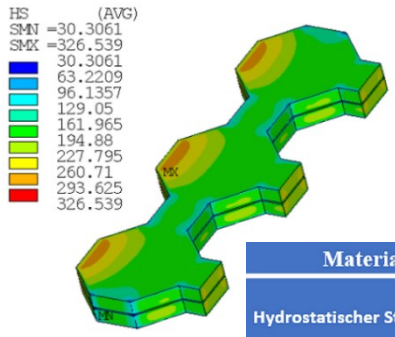
**Verena.Hein@xfab.com*

Introduction

The comparison of the electro migration performance and mechanical stability of AlCu, Ag, Au, Cu and Pt- highly robust metal tracks is necessary to evaluate materials for new medical and automotive applications. The possibilities to generate test results for thick and or noble metals are limited because of long test times, interacting of different failure mechanisms and material combinations. Simulations can support the choice of materials by values for mechanical stress and stress divergences [1, 2, 3, 4].

Simulation Results for Different Materials

The poster will present a study about the mechanical properties of different materials (Al, Ag, Au, Cu and Pt) for the highly robust layout for medical and automotive applications under electro migration stress conditions (Fig. 1).



Materials	AL	AG	AU	CU	PT(250)	PT(200)
Hydrostatischer Stress [MPa]	326.539	294.962	253.078	322.955	210.181	209.015

Figure 1. Stress distribution under applied stress current for the thick AlCu sandwich track and table for (Al, Ag, Au, Cu, Pt).

Conclusion

The positive influence of the highly robust metallization on the reliability performance of different thick and top metal metallizations depends on the used interconnect material. The use of the ANSYS simulation is very efficient to understand the differences in the mechanical as well as EM behavior.

Acknowledgements

The study is funded by the project iRel40 Intelligent Reliability 4.0 received funding from the ECSEL JOINT UNDERTAKING (JU) under grant agreement No 876659.

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P3

Micromechanical in-situ studies of on-chip interconnect stack structures using X-ray microscopy

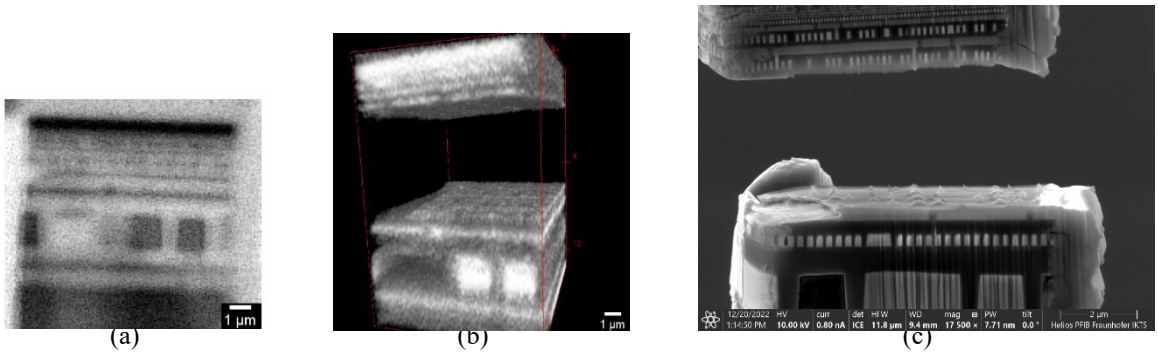
Stefan Weitz[1,2]*, André Clausner[2], Birgit Jost[2], Ehrenfried Zschech[3]

[1]*Fraunhofer Institute for Ceramic Technologies and Systems IKTS, Maria-Reiche-Str. 2, 01109 Dresden, Germany*
[2]*Brandenburg University of Technology Cottbus-Senftenberg, Konrad-Zuse-Str. 1, 03044 Cottbus, Germany*
[3]*deepXscan GmbH, Zeppelinstr. 1, 01324 Dresden, Germany*

**E-mail: Stefan.weitz@ikts.fraunhofer.de*

Semiconductor industry is continuing the scaling down of device structures and also of on-chip interconnect dimensions, both from performance reasons but also from economic reasons, to minimize the needed die size. This trend has implications for the design of guard ring structures, i.e. metallic non-functional structures in the back end of line (BEoL) stack at the periphery of these microchips. On the one hand, these metallic structures have to be designed to be efficient to stop microcracks and, on the other hand, the footprint of these structures has to be as small as possible. In this work, we present an in-situ experiment to study mechanical degradation and failure mechanisms in the BEoL stack, to ensure the mechanical robustness of microchips for future technology nodes.

To examine the effects of mechanical loading on the BEoL stack, a novel micromechanical in-situ experiment was integrated into an X-ray microscope (ZEISS Xradia 800 Ultra). This experimental setup enables high resolution imaging of the 3D-patterned sample structures and defects such as microcracks in 2D and 3D with a resolution of up to 50 nm during in-situ testing. Performing tomographies allows non-destructive 3D visualization of the interior throughout the entire experiment and thus 3D tracking of the microcrack during the whole duration. A suitable sample geometry was developed which allows the application of a tensile load to a BEoL specimen by a lever mechanism. The lever was actuated by a microindenter whose indentation force is simultaneously quantified by the setup. The intended cracking at a notch placed in the layered structure was verified by experimental testing, see 2D radiograph in Fig. 1(a) and post-mortem reconstructed 3D volume of the specimen in Fig. 1(b). The outcome was validated by SEM imaging, confirming planar microcrack propagation from the notch through the silicon and its copper via structures, see Fig. 1(c).



(a) (b) (c)

Figure 1. (a) 2D radiograph of the BEoL specimen prior the in-situ tensile test; (b) 3D reconstruction of the broken stack; (c) SEM image for the validation of the failed structure.

Acknowledgments

The authors would like to thank Kristina Kutukova, deepXscan GmbH Dresden, Germany, for helpful discussions.

Characterization of the thermo-mechanical behavior of Cu metallization in microelectronic applications

Michael Reisinger,[1]*, Sebastian Moser[1], Manuel Kleinbichler[2], Kostya Hlushkoa[3], Tobias Ziegelwanger[3], Jozef Keckes[3],

[1]*KAI Kompetenzzentrum Automobil- u. Industrieelektronik GmbH, Europastraße 8, 9524 Villach, Austria*
[2]*Infineon Technologies Austria AG, Siemensstraße 2, 9500 Villach, Austria*
[3]*Department of Materials Physics, Montanuniversitaet Leoben, Franz Josef-Straße 18, 8700 Leoben, Austria*

**michael.reisinger@k-ai.at*

In microelectronic industry, the basic understanding of the thermo-mechanical behavior of Cu metallization layers is crucial for lifetime modeling and the development of new devices. Such devices are complex structures, consisting of different materials, which undergo cyclic thermal loading caused by short circuit events during application. Due to mismatches of the thermal expansion coefficient, large thermo-mechanical stresses arise within the individual sublayers. Consequently, cyclic loading leads to degradation of the Cu metallization and at a certain stage might result into a loss of device functionality.

In this contribution dedicated test chips were used to study the fatigue behavior of Cu metallization layers during thermal cycling with application relevant heating rates of about 10^6 K/s. A variation of the loading parameters, such as heating rate, temperature range as well as repetition rate enables the investigation of the underlying physical mechanism. Complementary in-situ 20 kHz X-ray diffraction measurements were performed at the MS-Powder beamline of PSI. These experiments reveal the thermal stress in the Cu metallization layer, even when testing at high heating rates.

A quantitative comparison of the time and temperature dependency on the thermal-stress and the subsequent Cu metallization degradation is presented.

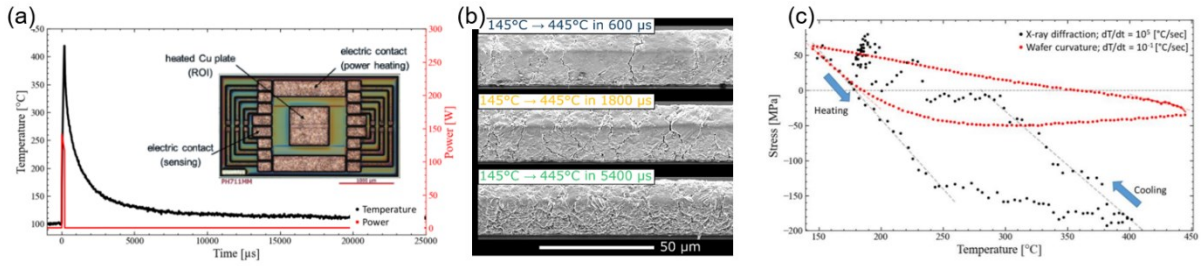


Figure 1. (a) Typical heating pulse and the corresponding test chip; (b) surface of Cu metallization lines after testing with different heating rates [1]; (c) Stress as a function of the temperature for different heating rates.

Acknowledgments

This work was funded by the Austrian Research Promotion Agency (FFG, Project No. 898207).

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Local gradients of microstructure and residual stresses in Si device side-walls separated by laser dicing

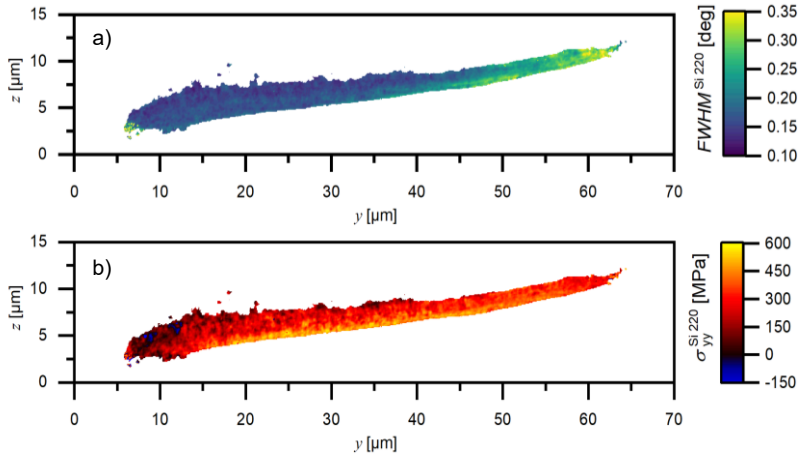
Tobias Ziegelwanger[1] *, Michael Meindlhumer[1], Juraj Todt[1], Michael Reisinger[2], Kurt Matoy[3], Jozef Keckes[1]

[1] *Chair of Materials Physics, Department Materials Science, Montanuniversität Leoben, Leoben, Austria*
[2] *KAI – Kompetenzzentrum Automobil- und Industrieelektronik GmbH, Villach, Austria*
[3] *Infineon Technologies AG, Villach, Austria*

**tobias.ziegelwanger@unileoben.ac.at*

The successful production of Si wafers with a diameter up to 12 inches and a small thickness of ~100 µm has led to the establishment of laser dicing as the primary tool for separation of individual chips. In order to provide high quality devices, manufacturers must take account of the heat affected zone as well as the redeposited layer grown by the ablated material. In general, investigations so far include transmission electron microscopy and 3-point bending to characterize the microstructure and mechanical strength [1]. In this contribution the local residual stress within the redeposited layer was quantified using cross-sectional X-ray nanodiffraction, performed at the synchrotron light source ESRF in Grenoble. Local gradients of residual stress and full width half maxima were evaluated between device front- and backside. Complementary characterization of microstructure in transmission electron microscopy could identify small metallic precipitations within the redeposited polycrystalline silicon layer as origin of these phenomena. It is assumed that this could impact the backside bending strength reported on in similar laser diced devices [2].

Figure 1. Local gradients of (a) residual stresses and (b) full width half maxima, from front side at 0 µm to the backside at 60 µm.



Acknowledgments
We acknowledge the European Synchrotron Radiation Facility for provision of beam time on ID13 and we would like to thank Dr. Amsa Medjahed for assistance. This work was funded by the Austrian Research Promotion Agency (FFG, Project No. 898207).

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P6

Investigating HCI and BTI degradation in 4H-SiC CMOS

André Lange[1]*, Sophie Winkler[1], Katrin Ortstein[1], Alexander May[2], Mathias Rommel[2]

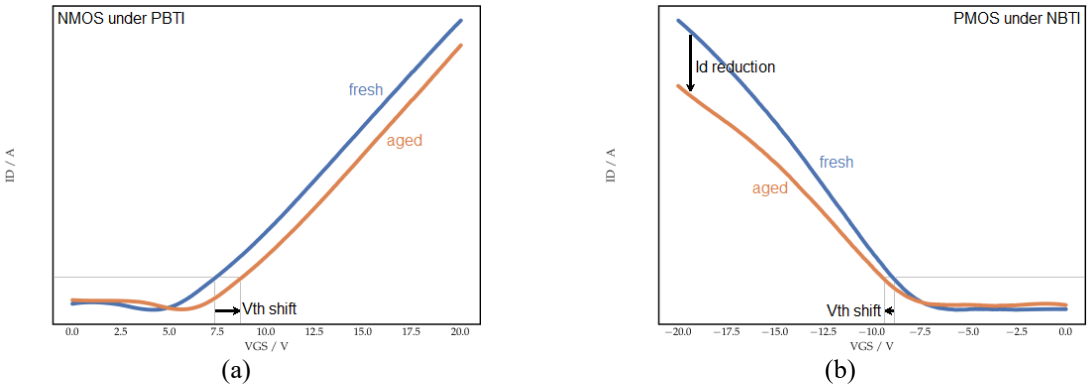
[1]*Fraunhofer Institute for Integrated Circuits IIS, Division Engineering of Adaptive Systems EAS; Münchner Straße 16, 01187 Dresden; Germany*
[2]*Fraunhofer Institute for Integrated Systems and Device Technology IISB; Schottkystrasse 10, 91058 Erlangen; Germany*

**andre.lange@eas.iis.fraunhofer.de*

Silicon is the dominating semiconductor material. However, under harsh environmental conditions, it approaches its limits while wide-bandgap semiconductors, such as silicon carbide (SiC), offer technological advantages, e.g. for space applications. Integrated circuits in the SiC technology of Fraunhofer IISB can currently be operated at temperatures up to ≥ 300 °C, and the technology is available to early adopters for their design projects [1].

Further developments of this technology will have to consider transistor reliability, since, as for silicon, integrated SiC field effect transistors (FET) suffer from degradation mechanisms. In a first experimental study based on a small number of test devices in an early technology version, we applied measurement principles known from silicon and applied them to characterizing the reliability of integrated SiC FETs. In particular, we investigated the impacts of hot carrier injection (HCI) and bias temperature instability (BTI) onto the behavior of SiC FETs. This approach is a good starting point but might need adaptations depending on how the technology capabilities and the application requirements evolve.

As a result, we see that for the examined technology, the transferability of Si methods to SiC seems to depend on the device type and the mechanism. Figure 1 refers to an NMOS device under positive BTI (PBTI) and a PMOS device under negative BTI (NBTI). The plots visualize transfer characteristics of fresh devices and the same devices after applying a sequence of stress and recovery. PBTI at the NMOS shifts the transfer characteristic towards higher gate-source voltages VGS, which corresponds to an increase of the threshold voltage Vth and fits the expectations from silicon [2]. NBTI at PMOS devices typically changes the shape of the transfer characteristics significantly, indicating that not only the threshold voltage Vth is affected by NBTI. Identifying root causes and implications as well as deriving countermeasures will be subject to future research.



(a) (b)

Figure 1. Transfer characteristics of test devices before (blue) and after (orange) a sequence of BTI stress and recovery. (a) NMOS under PBTI; (b) PMOS under NBTI

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P7

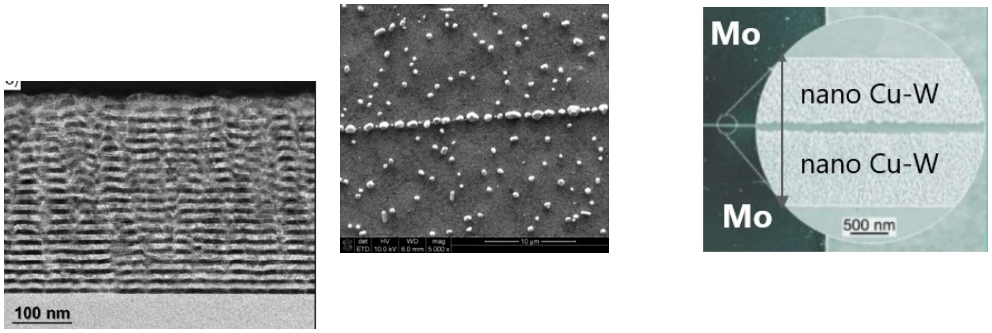
Nanomultilayers for thermal management and micro-/nano-joining

Jolanta Janczak-Rusch[1]*, Claudia Cancellieri, Jeyun Yeom, Bastian Rheingans, Lars P.H. Jeurgens

[1]*Empa, Swiss Federal Laboratories for Materials Science and Technology, Überlandstrasse 129, Dübendorf, CH-8600 Switzerland*

**jolanta.janczak-rusch@empa.ch*

The miniaturization and multifunctionalization of microelectronic requires new material and technology concepts. With this in mind, we are developing nanomultilayers (NMLs) that enable low-temperature joining processes while supporting the thermal management in high-packaging density devices. The NMLs (Fig.1a) consist of alternating nanolayers (individual thickness < 10 nm, total thickness < 1 μm) of a metal or metal alloy (e.g. Ag, Cu, Ag-Cu) and a chemically inert barrier material (e.g. refractory metal, nitride, carbon), and are deposited by magnetron sputtering. Our studies show that nanostructured metals in a multilayer configuration exhibit fast directional migration at comparatively low temperatures (Fig.1b), which can be utilized to significantly reduce the bonding temperature. Additionally, when using metallic nanomultilayers of immiscible metals such as Cu/W or Cu/Mo, nanocomposites with tailored thermal and mechanical properties can be formed in-situ during the joining processes (Fig. 1c). The unique and controlled thermal and mechanical properties of nanomultilayers open new opportunities for micro-/nano-joining technology and help address the recent challenges in the microelectronic sector.



(a) (b) (c)

Figure 1. (a) Cross section of as-deposited Ag/AlN nanomultilayer (SEM image) [1] (b) Planar view of annealed Ag/AlN nanomultilayer (SEM image): fast, intensive outward migration of Ag at temperature of 450 °C [1] (c) in-situ formation of Cu-W nanocomposite with tailored properties in a Mo-joint brazed at 750 °C [2].

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P8

Thin-film transfer by nanopaste sinter-bonding

Bastian Rheingans*, Fabio La Mattina, Jordan Bouaziz, Claudia Cancellieri, Lars P. H. Jeurgens, J. Janczak-Rusch

Empa, Swiss Federal Laboratories for Materials Science and Technology, Überlandstrasse 129, Dübendorf, CH-8600 Switzerland

**bastian.rheingans@empa.ch*

Transfer and integration of thin-film and 2D materials plays a crucial role for realizing novel applications, e.g. for sensing, catalysis, or flexible electronics. To maintain the unique properties of these materials, on the one hand film deterioration during lift-off, transfer, and re-attachment must be minimized. On the other hand, the bond between film and host substrate must withstand the respective operation conditions, e.g. elevated temperatures or harsh environments. In this regard, sinter-bonding with nanoparticle pastes (nanopastes) represents a promising method for thin-film transfer, since it allows creation of a firm and temperature-stable metallic bond in a comparatively gentle joining process.

As an example case, we present the transfer of epitaxial perovskite films by sinter-bonding with Ag-nanopaste, to be used at high temperatures in oxidative atmospheres (Figure 1; [1]): $SrRuO_3$ (SRO) and $SrTiO_3$ (STO) films with up to 180 nm thickness were grown by pulsed laser deposition on STO parent substrates at $T > 700$ °C. $Sr_3Al_2O_6$ (SAO) served as sacrificial interlayer that allows for epitaxial growth of SRO and STO and is soluble in water. For bonding, both films and Si host substrates were metallized with Au. Sinter-bonding was performed on a manual flip-chip bonder at 250 °C for 10 min. After dissolution of the SAO interlayer and removal of the parent substrate, the quality of the transferred epitaxial films was analyzed by optical and atomic force microscopy, as well as X-ray diffraction (stress analysis, rocking curves). The transferred films exhibited high flatness and no visible damage (cracks, buckling etc.), no significant change in stress state, and only slight increase in mosaicity. This indicates that film damage was largely avoided upon transfer. Cross-sectional analysis of the bonding zone showed a typical porous layer of sintered Ag, and formation of an Ag-Au solid solution at the interface between sintered Ag and transferred film. We believe that nanopaste-based transfer methods represent an important step towards advanced electronic integration of thin-film materials.

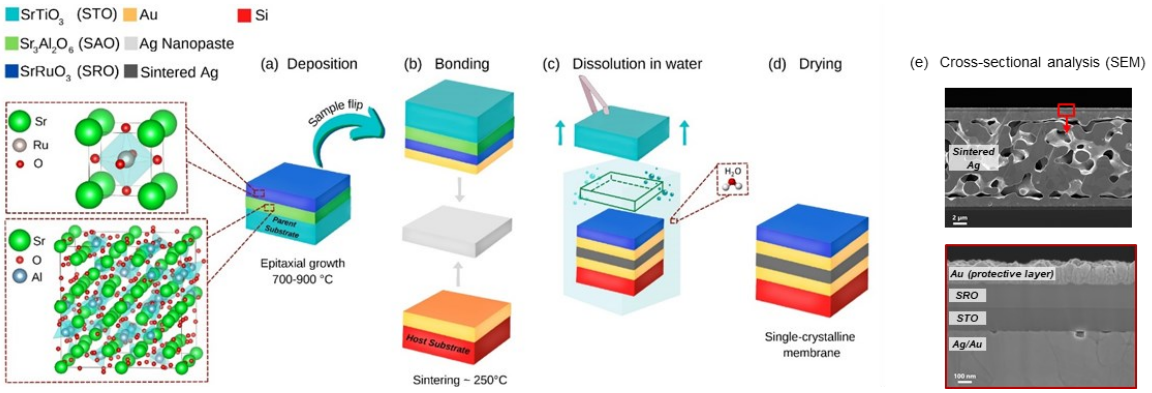

Figure 1. Thin-film transfer process and cross-section analysis (modified after [1]).

Acknowledgments

Internal funding from Empa (Internal Research Call 2020) is gratefully acknowledged.

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In-situ TEM study and nanomechanical characterization of fracture behavior in two-dimensional covalent organic frameworks

Bowen Zhang[1, 2] *, Zhongquan Liao[1], Xiaohui Liu[3], Wei Li[3], Ehrenfried Zschech[2,4]

[1]*Fraunhofer Institute for Ceramic Technologies and System (IKTS), Maria-Reiche-Straße 2, 01109, Dresden, Germany,*
[2]*Faculty of Electrical and Computer Engineering, Technische Universität Dresden, 01062, Dresden, Germany,*
[3]*Faculty of Chemistry and Food Chemistry, Technische Universität Dresden, 01062, Dresden, Germany,*
[4]*deepXscan GmbH, Zeppelinstr 1, D-01324 Dresden, Germany*

**Email: bowen.zhang@ikts-extern.fraunhofer.de*

Two-dimensional (2D) crystalline polymers, particularly covalent organic frameworks (COFs), have been emerging as a class of promising materials in electronics/optoelectronics, energy storage/conversion, gas separation and catalyst applications. They have a highly ordered covalently linked network along orthogonal directions, designable structures, and multifunctional properties for various application scenarios [1-5]. However, although the outstanding mechanical properties have been proved and they are envisioned to be core parts in flexible electronics [6-8], revealing the fracture behaviour and mechanism of 2D COFs at molecular level has not been realised yet while this knowledge is crucial and fundamental for tailoring their properties and to improve the mechanical reliability of flexible device. To this end, we demonstrate a detailed observation of fracture process in an imine-based 2D COF by *in-situ* tensile testing in transmission electron microscopy (TEM, Libra200, Carl Zeiss). By optimizing the transferring and patterning procedures, we report that a large elastic strain up to ~6.7% is achieved in 2D polyimine, with a corresponding elastic modulus of ~10.9 GPa. Furthermore, we observed the rough edge of propagated crack with branches and delamination. Trans-granular fracture is clearly visible which is contrary to expectation and previous research. Our *in-situ* experimental investigations can be furtherly elucidated by molecular dynamic simulation to provide in-depth insights into intrinsic fracture mechanisms of 2D COFs and pave the way for future flexible electronic applications.

Acknowledgments

Bowen Zhang acknowledges the financial support from China Scholarship Council (CSC). The authors also thank the technical support from J. Posseckardt and S. Conzendorf at Fraunhofer IKTS Dresden, Germany, for SEM operation, and Z.Y. Wang and J.J. Zhang at Faculty of Chemistry and Food Chemistry, Technische Universität Dresden, Germany, for sample preparation and transferring.

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Shaping the topography of solar wafers due to increased reactivity of lattice strained silicon

Thomas Langner[1*], Tim Sieber[1] and Jörg Acker[1]

[1]*Brandenburg University of Technology Cottbus-Senftenberg, Department of Physical Chemistry, 01968 Senftenberg, Germany*

* *E-Mail: thomas.langner@b-tu.de*

Multi-wire sawing using an abrasive SiC slurry or diamond wires constitute the main slicing techniques for multi- and monocrystalline silicon crystals in photovoltaics. The massive indentation of the abrasive SiC results in mechanical load during the sawing process and creates a wafer surface layer characterized by lattice defects, pits, fractures, rifts, cracks, amorphous Si and even some high-pressure Si modifications, otherwise known as saw damage.[1] This highly defect-rich surface causes the rapid recombination of electron-hole pairs, requiring that it be removed by etching in order to manufacture solar cells and to generate a surface morphology having a low reflectivity which directly affects the solar cell's efficiency.
Etching the surface layer using typical HF−HNO3− H2SiF6 acid mixtures leads to a heterogeneous and laterally unevenly distributed etch attack and a significantly higher etch rate compared to the underlying bulk silicon.[2,3] The present study is focused on the question of how mechanically introduced lattice strain in single-crystalline silicon alters the chemical reactivity of the silicon atoms affected by the strain field on a microscopic length scale. Scratches were introduced into single crystalline Si surfaces in model experiments, and the magnitude and local distribution of lattice strain were extracted from confocal Raman microscopy measurements according to Domnich et al..[4] One of the parameters used to describe the reactivity of silicon is the local etch rate, which was derived from the local removal before and after etching by confocal microscopy. Wet-chemical etching was performed with HF-HNO_3-H_2SiF_6 acid mixtures of different concentrations. It was found, that the reactivity of silicon increased linearly with the magnitude of lattice strain. In particular, an increase in tensile strain led to a higher increase in reactivity compared to the increase observed with growing compressive strain. The second decisive parameter is the reactivity of the etch mixture. Diluted acid mixtures with a low reactivity attack only the highest strained Si, whereas more concentrated and therefore more reactive acid mixtures are able to attack even slightly strained Si. Side effects, such as the behavior of amorphous or nanocrystalline Si and the generation of highly reactive intermediary species while etching, are discussed.
Based on the presented results the major features of saw damage etching and the formation of the final surface topography can be explained.

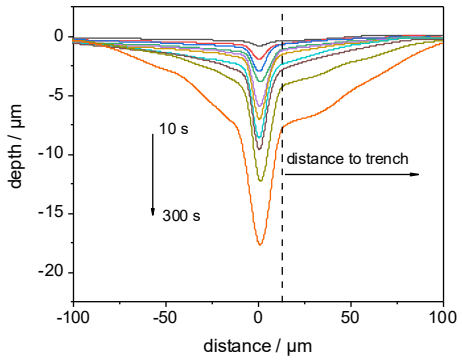

Figure 1. Time-dependent profile upgrowth of an acidic etched scratch

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Deposition of copper in lithium-ion batteries during the deep discharge process

Thomas Langner[1] *, Tim Sieber[1] and Jörg Acker[1]

[1]*Brandenburg University of Technology Cottbus-Senftenberg, Department of Physical Chemistry, 01968 Senftenberg, Germany*

* *E-Mail: thomas.langner@b-tu.de*

Spent lithium-ion batteries provide an important secondary raw material source of nickel, cobalt, manganese and lithium compounds to provide feedstock for the production of new cathode material. In a direct recycling process, such as functional recycling, each step of the process must be carried out in a way that avoids or reduces degradation products and impurities of the cathode material in order to directly use the recyclate for the production of new lithium-ion cells. The first step of recycling is always the deep discharge of the modules, in which the individual battery cells (pouch, prismatic, etc.) are electrically combined into one assembly unit, so that the lithium is transferred as far as possible into the cathode material to ensure safe disassembly of the cells. If cells with different charge capacities are connected in series, dissolution of the copper carrier foil and deposition of copper on the surface of the NMC cathode occurs in the cell with the lower charge capacity during deep discharge. When the anode is completely delithiated, no Li is available for further charge transport and the potential of the series-connected cells of higher charge capacity (SOC>0) represent the driving force to initiate charge transport through the copper of the anode in the cell of lower charge capacity, which is discharged at an earlier time (SOC=0), when the current flow continues (SOC<0). Based on measurements of the surface temperature, voltage drop, and copper concentration in the electrolyte during deep discharge of the cell, the dissolution point, onset of copper deposition, and formation of internal short circuits were identified, and a model of the processes during deep discharge was developed. Finally, the results show that series connection of cells with different states of charge leads to dissolution and deposition of copper and that dissolution of copper starts earlier than previously assumed. [1]

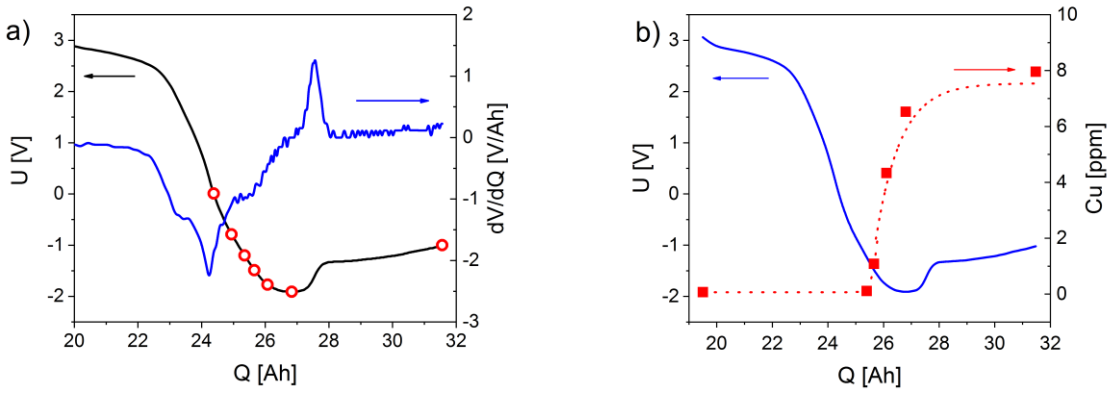

Figure 1. (a) discharge curve (black) of a cell during overdischarge, markings show the points of electrolyte removal, 1st derivative of the voltage curve (blue); (b) voltage curve of the cells during overdischarge; red dots show the copper concentration in the electrolyte

Acknowledgments

This research has been funded by the German Federal Ministry of Education and Research (BMBF) in the project "ReAlBatt" (project number 03XP0194D).

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P12

Degradation of Cathode Foils from Lithium-Ion Batteries in Humid Atmosphere

Thomas Langner[1*], Tim Sieber[1], Anja Rietig[1] and Jörg Acker[1]

[1]*Brandenburg University of Technology Cottbus-Senftenberg, Department of Physical Chemistry, 01968 Senftenberg, Germany*

* *E-Mail: thomas.langner@b-tu.de*

This poster deals with the chemical reactions that occur during the initial contact of a cathode foil from lithium-ion batteries. The adhering residues of the organic electrolyte and the conductive salt residues contained therein initiate processes that lead to the chemical dissolution of the aluminum carrier foil and significantly damage the cathode material. Cathodes made from used LiBs that have been stored in air for several days develop white, salt-like blooms on the surface of the NMC coating, which can reach typical diameters of 100...500 µm. At the same time, the cathode loses mechanical stability until it ultimately cracks under the slightest stress and disintegrates into flake-like pieces. If a cathode is decoated that already shows the first salt-like blooms on its surface, a large number of small holes become visible in the exposed Al carrier foil. To quantify the degradation, the relative ratio of the area of the holes formed, which increases with time, to the total area of the aluminum foil (AR) is determined by confocal microscopy. This shows that with increasing humidity, as well as with increasing duration, there is a greater extent of degradation in the form of holes.

The stoichiometric ratio between Al, O and S within the salt-like precipitate determined from the EDX images is n(Al):n(O):n(S) = (2.1 ± 0.1) : (4.8 ± 0.4) : (1.0 ± 0.1). To obtain information about the chemical composition of the crystallizates within the NMC coating, selected samples were analyzed using laser-induced breakdown spectroscopy (LIBS), which can also be used to detect lithium. LIBS analyses demonstrated that lithium and aluminum coexist in the crystalline precipitates on the cathode surface. In contrast, the LIBS depth profiles show that mainly aluminum is present in the individual ablation planes. By means of SEM-EDX as well as Raman microscopy, it could be shown that there are local degradation zones at the interface of the aluminum support foil and the NMC layer, in which characteristic Raman bands of the NMC are absent and the secondary particles are no longer recognizable.

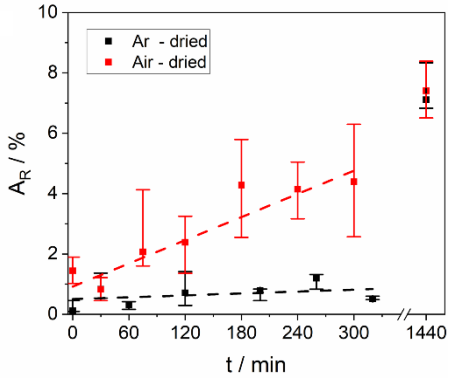

Figure 1. relative area of the holes of the foils during storage at ambient air humidity (ϕ ≈ 55%) as a function of time

Acknowledgments

This research has been funded by the Ministry of the Environment, Climate Protection and the Energy Sector Baden-Wuerttemberg in the project „DeMoBat“ (project number L7520106). LIBS measurements were taken by LTB Lasertechnik Berlin.

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